TYPICAL QUESTIONS & ANSWERS

PART - I

OBJECTIVE TYPE QUESTIONS

Each Question carries 2 marks.

Choose correct or the best alternative in the following:

Q.1 The NAND gate output will be low if the two inputs are
(A) 00 **(B)** 01
(C) 10 **(D)** 11

Ans: D
The NAND gate output will be low if the two inputs are 11
(The Truth Table of NAND gate is shown in Table.1.1)

X(Input)	Y(Input)	F(Output)
0	0	1
0	1	1
1	0	1
1	1	0

Table 1.1 Truth Table for NAND Gate

Q.2 What is the binary equivalent of the decimal number 368
(A) 101110000 **(B)** 110110000
(C) 111010000 **(D)** 111100000

Ans: A
The Binary equivalent of the Decimal number 368 is 101110000
(Conversion from Decimal number to Binary number is given in Table 1.2)

2	368		
2	184	---	0
2	92	---	0
2	46	---	0
2	23	---	0
2	11	---	1
2	5	---	1
2	2	---	1
2	1	---	0
	0	---	1

Table 1.2 Conversion from Decimal number to Binary number

Q.3 The decimal equivalent of hex number 1A53 is

(A) 6793 **(B)** 6739
(C) 6973 **(D)** 6379

Ans: B

The decimal equivalent of Hex Number 1A53 is 6739
(Conversion from Hex Number to Decimal Number is given below)

1	A	5	3	Hexadecimal
16^3	16^2	16^1	16^0	Weights

$$(1A53)_{16} = (1 X 16^3) + (10 X 16^2) + (5 X 16^1) + (3 X 16^0)$$
$$= 4096 + 2560 + 80 + 3$$
$$= 6739$$

Q.4 $(734)_8 = (\ )_{16}$

(A) C 1 D **(B)** D C 1
(C) 1 C D **(D)** 1 D C

Ans: D

$(734)_8 = (1\ D\ C)_{16}$

0001 | 1101 | 1100
1 D C

Q.5 The simplification of the Boolean expression $(\overline{\overline{A}\overline{B}\overline{C}}) + (\overline{A\overline{B}C})$ is

(A) 0 **(B)** 1
(C) A **(D)** BC

Ans: B

The Boolean expression is $(\overline{\overline{A}\overline{B}\overline{C}}) + (\overline{A\overline{B}C})$ is equivalent to 1

$$(\overline{\overline{A}\overline{B}\overline{C}}) + (\overline{A\overline{B}C}) = \overline{\overline{A}} + \overline{B} + \overline{\overline{C}} + \overline{A} + \overline{\overline{B}} + \overline{C} = A + \overline{B} + C + \overline{A} + B + \overline{C}$$
$$= (A+\overline{A})(B+\overline{B})(C+\overline{C}) = 1X1X1 = 1$$

Q.6 The number of control lines for a 8 – to – 1 multiplexer is

(A) 2 **(B)** 3
(C) 4 **(D)** 5

Ans: B

The number of control lines for an 8 to 1 Multiplexer is 3
(The control signals are used to steer any one of the 8 inputs to the output)

Q.7 How many Flip-Flops are required for mod–16 counter?

(A) 5 **(B)** 6
(C) 3 **(D)** 4

Ans: D

The number of flip-flops is required for Mod-16 Counter is 4.

(For Mod-m Counter, we need N flip-flops where N is chosen to be the smallest number for which 2N is greater than or equal to m. In this case 24 greater than or equal to 1)

Q.8 EPROM contents can be erased by exposing it to

(A) Ultraviolet rays. **(B)** Infrared rays.
(C) Burst of microwaves. **(D)** Intense heat radiations.

Ans: A

EPROM contents can be erased by exposing it to Ultraviolet rays
(The Ultraviolet light passes through a window in the IC package to the EPROM chip where it releases stored charges. Thus the stored contents are erased).

Q.9 The hexadecimal number 'A0' has the decimal value equivalent to

(A) 80 **(B)** 256
(C) 100 **(D)** 160

Ans: D

The hexadecimal number 'A0' has the decimal value equivalent to 160

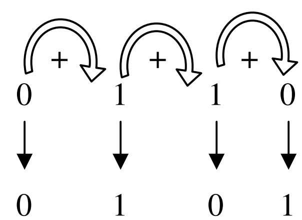
(A 0
16^1 16^0 $= 10X16^1 + 0X16^0 = 160$)

Q.10 The Gray code for decimal number 6 is equivalent to

(A) 1100 **(B)** 1001
(C) 0101 **(D)** 0110

Ans: C

The Gray code for decimal number 6 is equivalent to 0101
(Decimal number 6 is equivalent to binary number 0110)



Q.11 The Boolean expression $\overline{A}.B + A.\overline{B} + A.B$ is equivalent to

(A) $A + B$ **(B)** $\overline{A}.B$
(C) $\overline{A + B}$ **(D)** A.B

Ans: A

The Boolean expression $\overline{A}.B + A.\overline{B} + A.B$ is equivalent to A + B

$(\overline{A}.B + A.\overline{B} + A.B = B(\overline{A} + A) + A.\overline{B}$
$= B + A.\overline{B}$ $\{\because (\overline{A} + A) = 1\}$
$= A + B$ $\{\because (B + A.\overline{B}) = B + A\}$

Q.12 The digital logic family which has minimum power dissipation is

(A) TTL **(B)** RTL
(C) DTL **(D)** CMOS

Ans: D
The digital logic family which has minimum power dissipation is CMOS.
(CMOS being an unipolar logic family, occupy a very small fraction of silicon Chip area)

Q.13 The output of a logic gate is 1 when all its inputs are at logic 0. the gate is either
(A) a NAND or an EX-OR **(B)** an OR or an EX-NOR
(C) an AND or an EX-OR **(D)** a NOR or an EX-NOR

Ans: D
The output of a logic gate is 1 when all inputs are at logic 0. The gate is either a NOR or an EX-NOR .
(The truth tables for NOR and EX-NOR Gates are shown in fig.1(a) & 1(b).)

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

Fig.1(a) Truth Table for NOR Gate

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	1

Fig.1(b) Truth Table for EX-NOR Gate

Q.14 Data can be changed from special code to temporal code by using
(A) Shift registers **(B)** counters
(C) Combinational circuits **(D)** A/D converters.

Ans: A
Data can be changed from special code to temporal code by using Shift Registers.
(A Register in which data gets shifted towards left or right when clock pulses are applied is known as a Shift Register.)

Q.15 A ring counter consisting of five Flip-Flops will have
(A) 5 states **(B)** 10 states
(C) 32 states **(D)** Infinite states.

Ans: A
A ring counter consisting of Five Flip-Flops will have 5 states.

Q.16 The speed of conversion is maximum in
(A) Successive-approximation A/D converter.
(B) Parallel-comparative A/D converter.
(C) Counter ramp A/D converter.
(D) Dual-slope A/D converter.

Ans: B

The speed of conversion is maximum in Parallel-comparator A/D converter (Speed of conversion is maximum because the comparisons of the input voltage are carried out simultaneously.)

Q.17 The 2's complement of the number 1101101 is

(A) 0101110 **(B)** 0111110
(C) 0110010 **(D)** 0010011

Ans: D

The 2's complement of the number 1101101 is 0010011
(1's complement of the number 1101101 is 0010010
2's complement of the number 1101101is 0010010 + 1 =0010011)

Q.18 The correction to be applied in decimal adder to the generated sum is

(A) 00101 **(B)** 00110
(C) 01101 **(D)** 01010

Ans: B

The correction to be applied in decimal adder to the generated sum is 00110.
When the four bit sum is more than 9 then the sum is invalid. In such cases, add +6(i.e. 0110) to the four bit sum to skip the six invalid states. If a carry is generated when adding 6, add the carry to the next four bit group .

Q.19 When simplified with Boolean Algebra (x + y)(x + z) simplifies to

(A) x **(B)** x + x(y + z)
(C) x(1 + yz) **(D)** x + yz

Ans: D

When simplified with Boolean Algebra (x + y)(x + z) simplifies to x + yz
[(x + y) (x + z)] = xx + xz + xy + yz = x + xz + xy + yz (∵ xx = x)
= x(1+z) + xy + yz = x + xy + yz {∵ (1+z) = 1}
= x(1 + y) + yz = x + yz {∵ (1+y) = 1}]

Q.20 The gates required to build a half adder are

(A) EX-OR gate and NOR gate **(B)** EX-OR gate and OR gate
(C) EX-OR gate and AND gate **(D)** Four NAND gates.

Ans: C

The gates required to build a half adder are EX-OR gate and AND gate
Fig.1(d) shows the logic diagram of half adder.

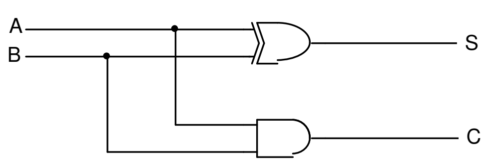


Fig.1(d) Logic diagram of Half Adder

Q.21 The code where all successive numbers differ from their preceding number by single bit is

(A) Binary code. **(B)** BCD.
(C) Excess – 3. **(D)** Gray.

Ans: D

The code where all successive numbers differ from their preceding number by single bit is Gray Code.

(It is an unweighted code. The most important characteristic of this code is that only a single bit change occurs when going from one code number to next.)

Q.22 Which of the following is the fastest logic

(A) TTL **(B)** ECL
(C) CMOS **(D)** LSI

Ans: B

ECL is the fastest logic family of all logic families.

(High speeds are possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated.

Q.23 If the input to T-flipflop is 100 Hz signal, the final output of the three T-flipflops in cascade is

(A) 1000 Hz **(B)** 500 Hz
(C) 333 Hz **(D)** 12.5 Hz.

Ans: D

If the input to T-flip-flop is 100 Hz signal, the final output of the three T-flip-flops in cascade is 12.5 Hz

{The final output of the three T-flip-flops in cascade is

$$(T) = \frac{Frequency}{2^N} = \frac{100}{2^3} = 12.5\text{Hz}\}$$

Q.24 Which of the memory is volatile memory

(A) ROM **(B)** RAM
(C) PROM **(D)** EEPROM

Ans: B

RAM is a volatile memory

(Volatile memory means the contents of the RAM get erased as soon as the power goes off.)

Q.25 -8 is equal to signed binary number

(A) 10001000 **(B)** 00001000
(C) 10000000 **(D)** 11000000

Ans: A

- 8 is equal to signed binary number 10001000

(To represent negative numbers in the binary system, Digit 0 is used for the positive sign and 1 for the negative sign. The MSB is the sign bit followed by the magnitude bits. i.e.,

\- 8 = 1000 1000

\-

Sign Magnitude

Q.26 DeMorgan's first theorem shows the equivalence of

(A) OR gate and Exclusive OR gate.
(B) NOR gate and Bubbled AND gate.
(C) NOR gate and NAND gate.
(D) NAND gate and NOT gate

Ans: B
DeMorgan's first theorem shows the equivalence of NOR gate and Bubbled AND gate
(Logic diagrams for De Morgan's First Theorem is shown in fig.1(a)

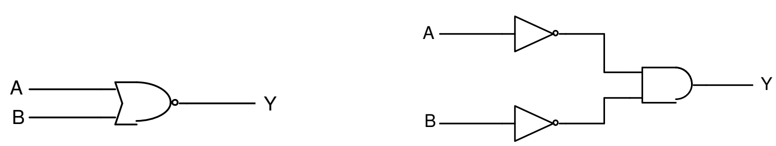


Fig.1(a) Logic Diagrams for De Morgan's First Theorem

Q.27 The digital logic family which has the lowest propagation delay time is

(A) ECL **(B)** TTL
(C) CMOS **(D)** PMOS

Ans: A
The digital logic family which has the lowest propagation delay time is ECL
(Lowest propagation delay time is possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated).

Q.28 The device which changes from serial data to parallel data is

(A) COUNTER **(B)** MULTIPLEXER
(C) DEMULTIPLEXER **(D)** FLIP-FLOP

Ans: C
The device which changes from serial data to parallel data is demultiplexer.
(A demultiplexer takes in data from one line and directs it to any of its N outputs depending on the status of the select inputs.)

Q.29 A device which converts BCD to Seven Segment is called

(A) Encoder **(B)** Decoder
(C) Multiplexer **(D)** Demultiplexer

Ans: B
A device which converts BCD to Seven Segment is called DECODER.
(A decoder coverts binary words into alphanumeric characters.)

Q.30 In a JK Flip-Flop, toggle means
(A) Set Q = 1 and $\overline{Q}$ = 0.
(B) Set Q = 0 and $\overline{Q}$ = 1.
(C) Change the output to the opposite state.
(D) No change in output.

Ans: C
In a JK Flip-Flop, toggle means Change the output to the opposite state.

Q.31 The access time of ROM using bipolar transistors is about
(A) 1 sec **(B)** 1 msec
(C) 1 μsec **(D)** 1 nsec.

Ans: C
The access time of ROM using bipolar transistors is about 1 μ sec.

Q.32 The A/D converter whose conversion time is independent of the number of bits is
(A) Dual slope **(B)** Counter type
(C) Parallel conversion **(D)** Successive approximation.

Ans: C
The A/D converter whose conversion time is independent of the Number of bits is Parallel conversion.
(This type uses an array of comparators connected in parallel and comparators compare the input voltage at a particular ratio of the reference voltage).

Q.33 When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero.
(A) Sign-magnitude. **(B)** 1's complement.
(C) 2's complement. **(D)** 9's complement.

Ans: A

Q.34 The logic circuit given below (Fig.1) converts a binary code $y_1y_2y_3$ into

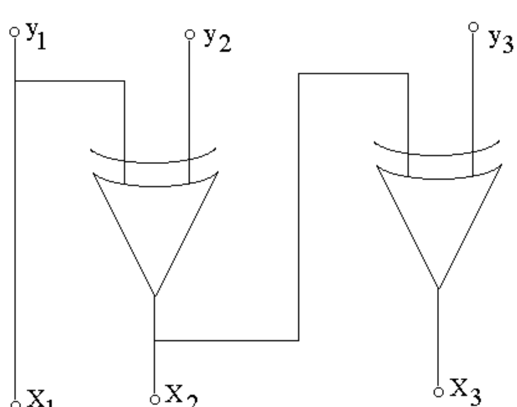


Fig.1

(A) Excess-3 code. **(B)** Gray code.
(C) BCD code. **(D)** Hamming code.

Ans: B

Gray code as

X1=Y1, X2=Y1 XOR Y2 , X3=Y1 XOR Y2 XOR Y3

For	Y1	Y2	Y3	X1	X2	X3
	0	0	0	0	0	0
	0	0	1	0	0	1
	0	1	0	0	1	1
	0	1	1	0	1	0

Q.35 The logic circuit shown in the given fig.2 can be minimised to

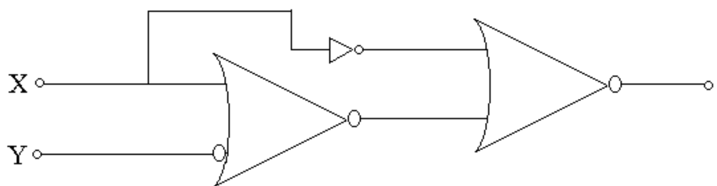
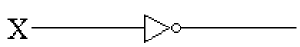
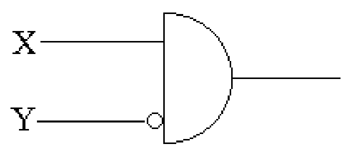


Fig.2

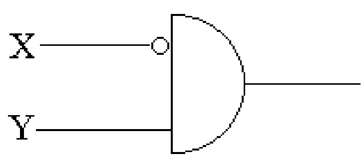
(A)



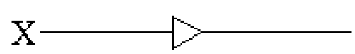
(B)



(C)



(D)



Ans: D

As output of the logic circuit is
Y=(X+Y')'+(X'+(X+Y')')'
(X+Y')'=X'Y Using DE Morgan's
Now this is one of input of 2nd gate.
F=(A+X')'=A'X=[(X'Y)'.X]
=[(X+Y')X]=X+XY'=X(Y')
=X

Q.36 In digital ICs, Schottky transistors are preferred over normal transistors because of their

(A) Lower Propagation delay. **(B)** Higher Propagation delay.
(C) Lower Power dissipation. **(D)** Higher Power dissipation.

Ans: A

Lower propagation delay as shottky transistors reduce the storage time delay by preventing the transistor from going deep into saturation.

Q.37 The following switching functions are to be implemented using a Decoder:

$f_1 = \sum m(1,2,4,8,10,14)$ $f_2 = \sum m(2,5,9,11)$ $f_3 = \sum m(2,4,5,6,7)$

The minimum configuration of the decoder should be

(A) 2 – to – 4 line. **(B)** 3 – to – 8 line.
(C) 4 – to – 16 line. **(D)** 5 – to – 32 line.

Ans: C

4 to 16 line decoder as the minterms are ranging from 1 to 14.

Q.38 A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be

(A) 15 ns. **(B)** 30 ns.
(C) 45 ns. **(D)** 60 ns.

Ans: A

15 ns because in synchronous counter all the flip-flops change state at the same time.

Q.39 Words having 8-bits are to be stored into computer memory. The number of lines required for writing into memory are

(A) 1. **(B)** 2.
(C) 4. **(D)** 8.

Ans: D

Because 8-bit words required 8 bit data lines.

Q.40 In successive-approximation A/D converter, offset voltage equal to $\frac{1}{2}$ LSB is added to the D/A converter's output. This is done to

(A) Improve the speed of operation.
(B) Reduce the maximum quantization error.
(C) Increase the number of bits at the output.
(D) Increase the range of input voltage that can be converted.

Ans: B

Q.41 The decimal equivalent of Binary number 11010 is

(A) 26. **(B)** 36.
(C) 16. **(D)** 23.

Ans: A

$11010 = 1 \text{ X } 2^4 + 1 \text{ X } 2^3 + 0 \text{ X } 2^2 + 1 \text{ X } 2^1 = 26$

Q.42 1's complement representation of decimal number of -17 by using 8 bit representation is

(A) 1110 1110 **(B)** 1101 1101
(C) 1100 1100 **(D)** 0001 0001

Ans: A

$(17)_{10} = (10001)_2$

In 8 bit = 00010001

1's Complement = 11101110

Q.43 The excess 3 code of decimal number 26 is

(A) 0100 1001 **(B)** 01011001
(C) 1000 1001 **(D)** 01001101

Ans: B

$(26)_{10}$ in BCD is (00100110) BCD

Add 011 to each BCD 01011001 for excess – 3

Q.44 How many AND gates are required to realize Y = CD+EF+G

(A) 4 **(B)** 5
(C) 3 **(D)** 2

Ans: D

To realize Y = CD + EF + G

Two AND gates are required (for CD & EF).

Q.45 How many select lines will a 16 to 1 multiplexer will have

(A) 4 **(B)** 3
(C) 5 **(D)** 1

Ans: A

In 16 to 1 MUX four select lines will be required to select 16 (2^4) inputs.

Q.46 How many flip flops are required to construct a decade counter

(A) 10 **(B)** 3
(C) 4 **(D)** 2

Ans: C

Decade counter counts 10 states from 0 to 9 (i.e. from 0000 to 1001)

Thus four FlipFlop's are required.

Q.47 Which TTL logic gate is used for wired ANDing

(A) Open collector output **(B)** Totem Pole
(C) Tri state output **(D)** ECL gates

Ans: A

Open collector output.

Q.48 CMOS circuits consume power

(A) Equal to TTL **(B)** Less than TTL
(C) Twice of TTL **(D)** Thrice of TTL

Ans: B

As in CMOS one device is ON & one is Always OFF so power consumption is low.

Q.49 In a RAM, information can be stored

(A) By the user, number of times.

(B) By the user, only once.
(C) By the manufacturer, a number of times.
(D) By the manufacturer only once.

Ans: A
RAM is used by the user, number of times.

Q.50 The hexadecimal number for $(95.5)_{10}$ is

(A) $(5F.8)_{16}$ **(B)** $(9A.B)_{16}$
(C) $(2E.F)_{16}$ **(D)** $(5A.4)_{16}$

Ans: A
$(95.5)_{10} = (5F.8)_{16}$

Integer part

16	95	
16	5	15 ↑
	0	5

Fractional part
0.5x16=8.0

Q.51 The octal equivalent of $(247)_{10}$ is

(A) $(252)_8$ **(B)** $(350)_8$
(C) $(367)_8$ **(D)** $(400)_8$

Ans: C
$(247)_{10} = (367)_8$

8	247	
8	30	↑7
8	3	6
	0	3

Q.52 The chief reason why digital computers use complemented subtraction is that it

(A) Simplifies the circuitry.
(B) Is a very simple process.
(C) Can handle negative numbers easily.
(D) Avoids direct subtraction.

Ans: C
Using complement method negative numbers can also be subtracted.

Q.53 In a positive logic system, logic state 1 corresponds to

(A) positive voltage **(B)** higher voltage level
(C) zero voltage level **(D)** lower voltage level

Ans: B

We decide two voltages levels for positive digital logic. Higher voltage represents logic 1 & a lower voltage represents logic 0.

Q.54 The commercially available 8-input multiplexer integrated circuit in the TTL family is

(A) 7495. **(B)** 74153.
(C) 74154. **(D)** 74151.

Ans: B
MUX integrated circuit in TTL is 74153.

Q.55 CMOS circuits are extensively used for ON-chip computers mainly because of their extremely

(A) low power dissipation. **(B)** high noise immunity.
(C) large packing density. **(D)** low cost.

Ans: C
Because CMOS circuits have large packing density.

Q.56 The MSI chip 7474 is

(A) Dual edge triggered JK flip-flop (TTL).
(B) Dual edge triggered D flip-flop (CMOS).
(C) Dual edge triggered D flip-flop (TTL).
(D) Dual edge triggered JK flip-flop (CMOS).

Ans: C
MSI chip 7474 dual edge triggered D Flip-Flop.

Q.57 Which of the following memories stores the most number of bits

(A) a $5M\times8$ memory. **(B)** a $1M \times 16$ memory.
(C) a $5M\times4$ memory. **(D)** a $1M\times12$ memory.

Ans: A
5Mx8 = 5 x 220 x 8 = 40M (max)

Q.58 The process of entering data into a ROM is called

(A) burning in the ROM **(B)** programming the ROM
(C) changing the ROM **(D)** charging the ROM

Ans: B
The process of entering data into ROM is known as programming the ROM.

Q.59 When the set of input data to an even parity generator is 0111, the output will be

(A) 1 **(B)** 0
(C) Unpredictable **(D)** Depends on the previous input

Ans: B
In even parity generator if number of 1 is odd then output will be zero.

Q.60 The number 140 in octal is equivalent to

(A) $(96)_{10}$. **(B)** $(86)_{10}$.
(C) $(90)_{10}$. **(D)** none of these.

Ans: A

$(140)_8 = (96)_{10}$

$1 \times 8^2 + 4 \times 8 + 0 \times 1 = 64 + 32 = 96$

Q.61 The NOR gate output will be low if the two inputs are

(A) 00 **(B)** 01
(C) 10 **(D)** 11

Ans: B, C, or D

O/P is low if any of the I/P is high

Q.62 Which of the following is the fastest logic?

(A) ECL **(B)** TTL
(C) CMOS **(D)** LSI

Ans: A

Q.63 How many flip-flops are required to construct mod 30 counter

(A) 5 **(B)** 6
(C) 4 **(D)** 8

Ans: A

Mod - 30 counter +/- needs 5 Flip-Flop as $30 < 2^5$
Mod - N counter counts total ' N ' number of states.
To count 'N' distinguished states we need minimum n FlipFlop's as $[N = 2^n]$
For eg. Mod 8 counter requires 3 Flip-Flop's $(8 = 2^3)$

Q.64 How many address bits are required to represent a 32 K memory

(A) 10 bits. **(B)** 12 bits.
(C) 14 bits. **(D)** 16 bits.

Ans: D

$32K = 2^5 \times 2^{10} = 2^{15}$,
Thus 15 address bits are required, Only 16 bits can address it.

Q.65 The number of control lines for 16 to 1 multiplexer is

(A) 2. **(B)** 4.
(C) 3. **(D)** 5.

Ans: B

As $16 = 2^4$, 4 Select lines are required.

Q.66 Which of following requires refreshing?

(A) SRAM. **(B)** DRAM.

(C) ROM. **(D)** EPROM.

Ans: B

Q.67 Shifting a register content to left by one bit position is equivalent to

(A) division by two. **(B)** addition by two.
(C) multiplication by two. **(D)** subtraction by two.

Ans:C

Q.68 For JK flip flop with J=1, K=0, the output after clock pulse will be

(A) 0. **(B)** 1.
(C) high impedance. **(D)** no change.

Ans: B

Q.69 Convert decimal 153 to octal. Equivalent in octal will be

(A) $(231)_8$. **(B)** $(331)_8$.
(C) $(431)_8$. **(D)** none of these.

Ans: A

$(153)_{10} = (231)_8$

8	153	1
8	19	3
8	2	2

Q.70 The decimal equivalent of $(1100)_2$ is

(A) 12 **(B)** 16
(C) 18 **(D)** 20

Ans: A

$(1100)_2 = (12)_{10}$

Q.71 The binary equivalent of $(FA)_{16}$ is

(A) 1010 1111 **(B)** 1111 1010
(C) 10110011 **(D)** none of these

Ans: B

$(FA)_{16} = (11111010)_{10}$

Q.72 The output of SR flip flop when S=1, R=0 is

(A) 1 **(B)** 0
(C) No change **(D)** High impedance

Ans: A

As for the SR flip-flop S=set input R=reset input ,when S=1, R=0, Flip-flop will be set.

Q.73 The number of flip flops contained in IC 7490 is

(A) 2. **(B)** 3.
(C) 4. **(D)** 10.

Ans: A

Q.74 The number of control lines for 32 to 1 multiplexer is

(A) 4. **(B)** 5.
(C) 16. **(D)** 6.

Ans: B

The number of control lines for 32 (2^5) and to select one input among them total 5 select lines are required.

Q.75 How many two-input AND and OR gates are required to realize Y=CD+EF+G

(A) 2,2. **(B)** 2,3.
(C) 3,3. **(D)** none of these.

Ans: A

Y=CD+EF+G
Number of two input AND gates=2
Number of two input OR gates = 2
One OR gate to OR CD and EF and next to OR of G & output of first OR gate.

Q.76 Which of following can not be accessed randomly

(A) DRAM. **(B)** SRAM.
(C) ROM. **(D)** Magnetic tape.

Ans: D

Magnetic tape can only be accessed sequentially.

Q.77 The excess-3 code of decimal 7 is represented by

(A) 1100. **(B)** 1001.
(C) 1011. **(D)** 1010.

Ans: D

An excess 3 code is always equal to the binary code +3

Q.78 When an input signal A=11001 is applied to a NOT gate serially, its output signal is

(A) 00111. **(B)** 00110.
(C) 10101. **(D)** 11001.

Ans: B

As A=11001 is serially applied to a NOT gate, first input applied will be LSB 00110.

Q.79 The result of adding hexadecimal number A6 to 3A is

(A) DD. **(B)** E0.
(C) F0. **(D)** EF.

Ans: B

Q.80 A universal logic gate is one, which can be used to generate any logic function. Which of the following is a universal logic gate?

(A) OR **(B)** AND
(C) XOR **(D)** NAND

Ans: D
NAND can generate any logic function.

Q.81 The logic 0 level of a CMOS logic device is approximately

(A) 1.2 volts **(B)** 0.4 volts
(C) 5 volts **(D)** 0 volts

Ans: D
CMOS logic low level is 0 volts approx.

Q.82 Karnaugh map is used for the purpose of

(A) Reducing the electronic circuits used.
(B) To map the given Boolean logic function.
(C) To minimize the terms in a Boolean expression.
(D) To maximize the terms of a given a Boolean expression.

Ans: C

Q.83 A full adder logic circuit will have

(A) Two inputs and one output.
(B) Three inputs and three outputs.
(C) Two inputs and two outputs.
(D) Three inputs and two outputs.

Ans: D
A full adder circuit will add two bits and it will also accounts the carry input generated in the previous stage. Thus three inputs and two outputs (Sum and Carry) are there.

Q.84 An eight stage ripple counter uses a flip-flop with propagation delay of 75 nanoseconds. The pulse width of the strobe is 50ns. The frequency of the input signal which can be used for proper operation of the counter is approximately

(A) 1 MHz. **(B)** 500 MHz.
(C) 2 MHz. **(D)** 4 MHz.

Ans: A

Maximum time taken for all flip-flops to stabilize is 75ns x 8 + 50 = 650ns. Frequency of operation must be less than 1/650ns = 1.5 MHz.

Q.85 The output of a JK flipflop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the following conditions.
(A) By applying J = 0, K = 0 and using a clock.
(B) By applying J = 1, K = 0 and using the clock.
(C) By applying J = 1, K = 1 and using the clock.
(D) By applying a synchronous preset input.

Ans: C
Preset state of JK Flip-Flop =1
With J=1 K=1 and the clock next state will be complement of the present state.

Q.86 The information in ROM is stored
(A) By the user any number of times.
(B) By the manufacturer during fabrication of the device.
(C) By the user using ultraviolet light.
(D) By the user once and only once.

Ans: B

Q.87 The conversation speed of an analog to digital converter is maximum with the following technique.
(A) Dual slope AD converter.
(B) Serial comparator AD converter.
(C) Successive approximation AD converter.
(D) Parallel comparator AD converter.

Ans: D

Q.88 A weighted resistor digital to analog converter using N bits requires a total of
(A) N precision resistors. **(B)** 2N precision resistors.
(C) N + 1 precision resistors. **(D)** N – 1 precision resistors.

Ans: A

Q.89 The 2's complement of the number 1101110 is
(A) 0010001. **(B)** 0010001.
(C) 0010010. **(D)** None.

Ans: C
1's complement of 1101110 is = 0010001
Thus 2's complement of 1101110 is = 0010001 + 1 = 0010010

Q.90 The decimal equivalent of Binary number 10101 is
(A) 21 **(B)** 31
(C) 26 **(D)** 28

Ans: A

$1x2^4 + 0x2^3 + 1x2^2 + 0x2^1 + 1x2^0$

$= 16 + 0 + 4 + 0 + 1 = 21.$

Q.91 How many two input AND gates and two input OR gates are required to realize Y = BD+CE+AB

(A) 1, 1 **(B)** 4, 2
(C) 3, 2 **(D)** 2, 3

Ans: A

There are three product terms, so three AND gates of two inputs are required.
As only two input OR gates are available, so two OR gates are required to get the logical sum of three product terms.

Q.92 How many select lines will a 32:1 multiplexer will have

(A) 5. **(B)** 8.
(C) 9. **(D)** 11.

Ans: A

For 32 inputs, 5 select lines will be required, as $2^5 = 32$.

Q.93 How many address bits are required to represent 4K memory

(A) 5 bits. **(B)** 12 bits.
(C) 8 bits. **(D)** 10 bits.

Ans: B

For representing 4K memory, 12 address bits are required as

$4K = 2^2 \times 2^{10} = 2^{12}$ $(1K = 1024 = 2^{10})$

Q.94 For JK flipflop J = 0, K=1, the output after clock pulse will be

(A) 1. **(B)** no change.
(C) 0. **(D)** high impedance.

Ans: C

J=0, K=1, these inputs will reset the flip-flop after the clock pulse. So whatever be the previous output, the next state will be 0.

Q.95 Which of following are known as universal gates

(A) NAND & NOR. **(B)** AND & OR.
(C) XOR & OR. **(D)** None.

Ans: A

NAND & NOR are known as universal gates, because any digital circuit can be realized completely by using either of these two gates.

Q.96 Which of the following memories stores the most number of bits

(A) $64K \times 8$ memory. **(B)** $1M \times 8$ memory.

(C) $32M \times 8$ memory. **(D)** 64×6 memory.

Ans: C

32M x 8 stores most number of bits

2^5 x 2^{20} = 2^{25} (1M = 2^{20} = 1K x 1K = 2^{10} x 2^{10})

Q.97 Which of following consume minimum power

(A) TTL. **(B)** CMOS.

(C) DTL. **(D)** RTL.

Ans: B

CMOS consumes minimum power as in CMOS one p-MOS & one n-MOS transistors are connected in complimentary mode, such that one device is ON & one is OFF.

PART – II

NUMERICALS

Q.1 Convert the octal number 7401 to Binary. **(4)**

Ans:

Conversion of Octal number 7401 to Binary:

Each octal digit represents 3 binary digits. To convert an octal number to binary number, each octal digit is replaced by its 3 digit binary equivalent shown below.

7	4	0	1
↓	↓	↓	↓
111	100	000	001

Thus, $(7401)_8 = (111100000001)_2$

Q.2 Find the hex sum of $(93)_{16} + (DE)_{16}$. **(4)**

Ans:

Hex Sum of $(93)_{16} + (DE)_{16}$

Convert Hexadecimal numbers 93 and DE to its binary equivalent shown below:-

93 → 10010011
DE → 11011110

101110001 → 171

Thus $(93)_{16} + (DE)_{16} = (171)_{16}$

Q.3 Perform 2's complement subtraction of $(7)_{10} - (11)_{10}$. **(4)**

Ans:

2's Complements Subtraction of $(7)_{10} - (11)_{10}$

First convert the decimal numbers 7 and 11 to its binary equivalents.

$(7)_{10} = (0111)_2$

$(11)_{10} = (1011)_2$ in 4-bit system

Then find out the 2's complement for 1011 i.e.,

1's Complement of 1011 is 0100

2's Complement of 1011 is 0101

So, $(7)_{10} - (11)_{10}$ = 0111
0101

1100

Since there is no carry over flow occurring in the summation, the result is a negative number, to find out its magnitude, 2's Complement of the result must be found.

2's Complement of 1100 is 0011

```
           1
    --------
        0100
    --------
```

Here the answer is $(-4)_{10}$ (or) in 2's complement it is 1100.

Q.4 What is the Gray equivalent of $(25)_{10}$. **(2)**

Ans:

Gray equivalent of $(25)_{10}$

The binary equivalent of Decimal number 25 is $(00100101)_2$

1. The left most bit (MSB) in gray code is the same as the left most in binary
2. Add the left most bit to the adjacent bit
3. Add the next adjacent pair and so on., Discard if we get a carry.

```
0 + 0 + 1 + 0 + 0 + 1 + 0 + 1
↓   ↓   ↓   ↓   ↓   ↓   ↓   ↓
0   0   1   1   0   1   1   1  ←—— Gray Number
```

Q.5 Evaluate x = $\overline{A}.B + C(\overline{A.D})$ using the convention A = True and B = False. **(4)**

Ans:

Evaluate x = $\overline{A}.B + C(\overline{A.D})$

$= \overline{A}B + C(\overline{A} + \overline{D})$ (Since $\overline{A.D} = \overline{A} + \overline{D}$ by using Demorgan's Law)

$= \overline{A}.B + C.\overline{A} + C.\overline{D}$

By using the given convention, A = True = 1; B = False = 0

$= \overline{1}.0 + C.\overline{1} + C.\overline{D} = 0 + 0 + C.\overline{D} = C.\overline{D}$

Q.6 Simplify the Boolean expression F = C(B + C)(A + B + C). **(6)**

Ans:

Simplify the Boolean Expression F = C (B +C) (A+B+C)

F = C (B+C) (A+B+C)

= CB + CC [(A+B+C)]

= CB + C [(A+B+C)] (∵ CC = C)

= CBA + CBB + CBC + CA + CB + CC

= ABC + CB + CB + CA + CB + CC (∵ CBB =CB & CBC = CB)

= ABC + CB + CA + C (∵ CB+CB+CB = CB; CC = C)

= ABC + BC + C (1+A)

= ABC + BC + C (∵ 1+A = 1)

= ABC + C (1+B)

$= ABC + C \quad (\because\ 1+B = 1)$
$= C\,(1+AB) = C\ \{\because (1+AB)=1\}$

Q.7 Simplify the following expression into sum of products using Karnaugh map $F(A,B,C,D) = \sum(1,3,4,5,6,7,9,12,13)$ **(7)**

Ans:
Simplification of the following expression into sum of products using Karnaugh Map:

$F(A,B,C,D) = \Sigma\,(1,3,4,5,6,7,9,12,13)$
Karnaugh Map for the expression $F(A,B,C,D) = \Sigma\,(1,3,4,5,6,7,9,12,13)$ is shown in Fig.4(a). The grouping of cells is also shown in the Figure.

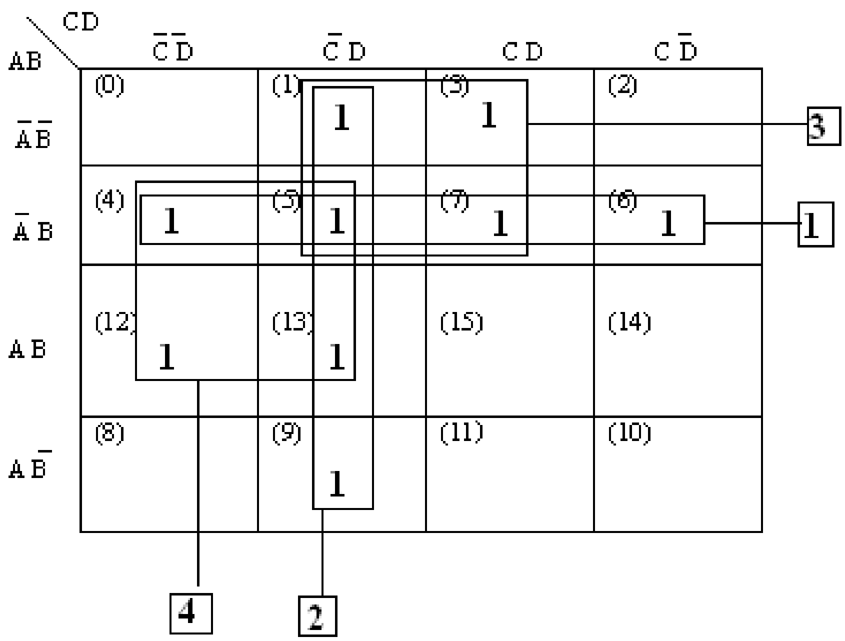


Fig 4(a)

The equations for (1) is $\bar{A}B$; (2) is $\bar{C}D$; (3) is $\bar{A}D$; (4) is $B\bar{C}$

Hence, the Simplified Expression for the above Karnaugh map is
$F(A,B,C,D) = \bar{A}B + \bar{C}D + \bar{A}D + B\bar{C}$
$= \bar{A}(B + D) + \bar{C}\,(B + D)$

Q.8 Simplify and draw the logic diagram for the given expression
$F = \overline{ABC} + \overline{AB}C + \overline{A}B\overline{C} + A\overline{BC} + A\overline{B}C.$ **(7)**

Ans:
Simplification of the logic expression
$F = \overline{ABC} + \overline{AB}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{BC} + A\,\overline{B}\,C$
$F = \overline{ABC} + \overline{AB}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{BC} + A\,\overline{B}\,C$

$F = \overline{A}+\overline{B}+\overline{C} + (\overline{A}+\overline{B})C + \overline{A}B\overline{C} + A(\overline{B}+\overline{C}) + A\overline{B}C$

$(\because \overline{ABC} = \overline{A}+\overline{B}+\overline{C}$ and $\overline{AB} = \overline{A}+\overline{B}$ by using Demorgan's Law)

$= \overline{A}+\overline{B}+\overline{C}+\overline{A}C+\overline{B}C+\overline{A}B\overline{C}+A\overline{B}+A\overline{C}+A\overline{B}C$

$=\overline{A}+\overline{A}C+\overline{B}+\overline{B}C+\overline{C}+A\overline{C}+\overline{A}B\overline{C}+A\overline{B}+A\overline{B}C$

$= \overline{A}(1+C)+\overline{B}(1+C)+\overline{C}(1+A)+\overline{A}B\overline{C}+A\overline{B}+A\overline{B}C$

$= \overline{A}+\overline{B}+\overline{C}+\overline{A}B\overline{C}+A\overline{B}+A\overline{B}C\ \{\because (1+C)=1 \text{ and } (1+A)=1\}$

$= (\overline{A}+A\overline{B})+\overline{B}(1+AC)+\overline{C}(1+\overline{A}B)$

$= (\overline{A}+\overline{B})+\overline{B}+\overline{C}\ \ \{\because (\overline{A}+A\overline{B}) = (\overline{A}+\overline{B});\ (1+AC)=1 \text{ and } (1+\overline{A}B)=1\}$

$F = (\overline{A}+\overline{B}+\overline{C})\ (\because \overline{B}+\overline{B}=\overline{B})$

The logic diagram for the simplified expression $F = (\overline{A}+\overline{B}+\overline{C})$ is given in fig.5(a)

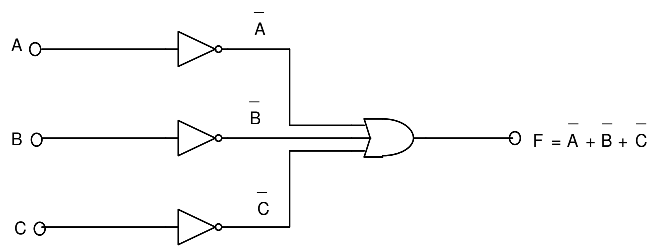


Fig.5(a) Logic diagram for the expression F = $(\overline{A}+\overline{B}+\overline{C})$

Q.9 Determine the binary numbers represented by the following decimal numbers. **(6)**
(i) 25.5 (ii) 10.625 (iiii) 0.6875

Ans:

(i) Conversion of decimal number 25.5 into binary number:

Here integer part is 25 and fractional part is 0.5. First convert the integer part 25 into its equivalent binary number i.e., divide 25 by 2 till the quotient becomes 0 shown in table 2(a)

	Quotient	Remainder
$\frac{25}{2}$	12	1
$\frac{12}{2}$	6	0
$\frac{6}{2}$	3	0
$\frac{3}{2}$	1	1
$\frac{1}{2}$	0	1

Table 2(a)

So, integer part $(25)_{10}$ is equivalent to the binary number 11001. Next convert fractional part 0.5 into binary form i.e., multiply the fractional part 0.5 by 2 till you get remainder as 0

0.5
X 2

1.0 ← Remainder
↓
1 (Quotient)

The decimal fractional part 0.5 is equivalent to binary number 0.1. Hence, the decimal number 25.5 is equal to the binary number 11001.1

(ii) Conversion of decimal number 10.625 into binary number:

Here integer part is 10 and fractional part is 0.625. First convert the decimal number 10 into its equivalent binary number i.e., divide 10 by 2 till the quotient becomes 0 shown in table 2(b)

	Quotient	Remainder
$\frac{10}{2}$	5	0
$\frac{5}{2}$	2	1 ↑
$\frac{2}{2}$	1	0
$\frac{1}{2}$	0	1

Table 2(b)

So, the integer part 10 is equal to binary number 1010. Next convert the decimal fractional part 0.625 into its binary form i.e., multiply 0.625 by 2 till the remainder becomes 0

0.625 → 0.250 → 0.50
X 2	X 2	X 2
1.250	0.50	1.0 ← (Remainder)
↓	↓	↓
1	0	1 ← (Quotient)
→

So, the decimal fractional part 0.625 is equal to binary number 0.101. Hence the decimal number **10.625** is equal to binary number **1010.101**.

(iii)Conversion of fractional number 0.6875 into its equivalent binary number:

Multiply the fractional number 0.6875 by 2 till the remainder becomes 0 i.e.,

0.6875 X 2	0.3750 X 2	0.75 X 2	0.5 X 2	
1.3750	0.75	1.5	1.0	← (Remainder)
1	0	1	1	← (Quotient)

So, the decimal fractional number **0.6875** is equal to binary number **0.1011**.

Q.10 Perform the following subtractions using 2's complement method. **(8)**
(i) 01000 – 01001 (ii) 01100 – 00011 (iii) 0011.1001 – 0001.1110

Ans:
(i) Subtraction of 01000-01001: 1's complement of 01001 is 10110 and 2's complement is
10110+ 1 =10111. Hence

```
  01000 =   01000
- 01001 =  +10111    (2's complement)
-------------------------
            11111    (Summation)
-------------------------
```

Since the MSB of the sum is 1, which means the result is negative and it is in 2's complement form. So, 2's complement of 1111 =00001= $(1)_{10}$. Therefore, the result is – 1.

(ii) Subtraction of 01100-00011: 1's complement of 00011 is 11100 and 2's complement is 11100 + 1 = 11101. Hence

```
  01100   =   01100
– 00011   = + 11101 (2's complement)
------------------------------------------
            1 01001 = + 9
            ↑
          Ignore
------------------------------------------
```

If a final carry is generated discard the carry and the answer is given by the remaining bits Which is positive i.e., $(1001)_2 = (+9)_{10}$

(iii) Subtraction of 0011.1001 – 0001.1110: 1's complement of 0001.1110 is 1110.0001 and its 2's complement is 1110.0010.

```
  0011.1001  =   0011.1001
- 0001.1110  = + 1110.1011 (2's complement)
------------------------------------------
           1 0001.101I = + 1 .68625
           ↑
         Ignore
```

If a final carry is generated discard the carry and the answer is given by the remaining bits which is positive i.e., $(0001.1011)_2 = (+\,1.68625)_{10}$

Q.11 Simplify the expressions using Boolean postulates **(9)**

(i) $\overline{\overline{X\overline{Y} + XYZ} + X(Y + X\overline{Y})}$ **(ii)** Y = (A + B)($\overline{A}$ + C)(B + C)

(iii) XY + $\overline{XZ}$ + X$\overline{Y}$Z (XY + Z)

Ans:

(i) $\overline{\overline{X\overline{Y} + XYZ} + X(Y + X\overline{Y})}$

$= \overline{\overline{X\overline{Y} + XYZ} + X(Y + X\overline{Y})}$

$= \overline{\overline{X(\overline{Y} + YZ)} + X(Y + X\overline{Y})}$

$= \overline{\overline{X(\overline{Y} + Z)} + X(Y + X)}$

(Because $\overline{Y} + YZ = \overline{Y} + Z$ and $Y + X\overline{Y} = Y + X$)

$= \overline{\overline{X\overline{Y} + XZ} + XY + XX}$

$= \overline{\overline{X\overline{Y} + XZ} + XY + X}$ (Because XX=X)

$= \overline{\overline{X\overline{Y} + XZ} + X(1 + Y)}$

$= \overline{\overline{X\overline{Y} + XZ} + X}$ (Because (1+Y=1)

$= \overline{(\overline{X} + Y)(\overline{X} + \overline{Z}) + X}$ (Because $\overline{XY} = \overline{X} + \overline{Y}$)

$= \overline{\overline{X}\,\overline{X} + \overline{X}\,\overline{Z} + Y\overline{X} + Y\overline{Z} + X}$

$= \overline{\overline{X} + \overline{X}\,\overline{Z} + Y\overline{X} + Y\overline{Z} + X}$ (Because $\overline{X}\,\overline{X} = \overline{X}$)

$= \overline{\overline{X}(1 + \overline{Z} + Y) + Y\overline{Z} + X}$

$= \overline{\overline{X} + Y\overline{Z} + X}$

$= \overline{(\overline{X} + X) + Y\overline{Z}}$

$= \overline{1 + Y\overline{Z}}$ (Because $\overline{X} + X = 1$)

$= \overline{1} = 0$ (Because $1 + Y\overline{Z} = 1$)

(ii) Y = (A + B)($\overline{A}$ + C)(B + C)

Y = (A + B)($\overline{A}$ + C)(B + C)

= (A$\overline{A}$ + AC + B$\overline{A}$ + BC) (B + C)

= (AC + B$\overline{A}$ + BC) (B + C) (Because A$\overline{A}$ = 0)

= ABC + BB$\overline{A}$ + BBC + ACC + B$\overline{A}$C + BCC

= ABC + B$\overline{A}$ + BC + AC + B$\overline{A}$C + BC (Because BB = B)

= ABC + AC + B$\overline{A}$ + B$\overline{A}$C + BC (Because BC + BC = BC)

=AC (B+1) + B$\overline{A}$ + BC ($\overline{A}$+1)

= AC + B$\overline{A}$ + BC (Because B + 1 = 1 and $\overline{A}$ + 1 = 1)

= AC + B$\overline{A}$ + BC (A + $\overline{A}$) (Because A + $\overline{A}$ = 1)

= AC + B$\overline{A}$ + BCA + BC$\overline{A}$

= AC(1 + B) + B$\overline{A}$(1 + C)

$= AC + B\bar{A}$ {Because (1 + B) = 1 and (1 + C) =1}

(iii) $XY + \overline{XZ} + X\bar{Y}Z\,(XY + Z)$

$= XY + \overline{XZ} + X\bar{Y}Z\,(XY + Z)$

$= XY + \overline{XZ} + XXY\bar{Y}Z + X\bar{Y}ZZ$

$= XY + \overline{XZ} + X\bar{Y}Z$ (Because $Y\bar{Y} = 0$ & $ZZ = Z$)

$= XY + \bar{X} + \bar{Z} + X\bar{Y}Z$ (Because $\overline{XZ} = \bar{X} + \bar{Z}$)

$= \bar{X} + XY + \bar{Z} + X\bar{Y}Z$

$= \bar{X} + X\,(Y + \bar{Y}Z) + \bar{Z}$

$= \bar{X} + X\,(Y + Z) + \bar{Z}$ (Because $Y + \bar{Y}Z = Y + Z$)

$= \bar{X} + X\,Y\,(Z + \bar{Z}) + XZ + \bar{Z}$ (Because $Z + \bar{Z} = 1$)

$= \bar{X} + X\,Y\,Z + XY\bar{Z} + XZ + \bar{Z}$

$= \bar{X} + XZ\,(1 + Y) + \bar{Z}\,(1 + XY)$

$= \bar{X} + XZ + \bar{Z}$ (Because $1 + Y = 1$ & $1 + XY = 1$)

$= \bar{X} + XZ) + \bar{Z}$

$=(\bar{X} + Z) + \bar{Z}$ (Because $\bar{X} + XZ = \bar{X} + Z$

$= \bar{X} + (Z + \bar{Z})$

$= \bar{X} + 1$ (Because $Z + \bar{Z} = 1$)

$=1$ (Because $\bar{X} + 1 = 1$)

Q.12 Minimize the logic function $Y(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$. Use Karnaugh map. Draw logic circuit for the simplified function. **(9)**

Ans:

Fig. 4(a) shows the Karnaugh map. Since the expression has 4 variables, the map has 16 cells. The digit 1 has been written in the cells having a term in the given expression. The decimal number has been added as subscript to indicate the binary number for the concerned cell. The term $ABC\bar{D}$ cannot be combined with any other cell. So this term will appear as such in the final expression. There are four groupings of 4 cells each. These correspond to the min terms (0, 1, 2, 3), (0, 1, 8, 9), (1, 3,5,7) and (1, 3, 9, 11). These are shown in the map. Since all the terms (except 14) have been included in groups of 4 cells, there is no need to form groups of two cells.

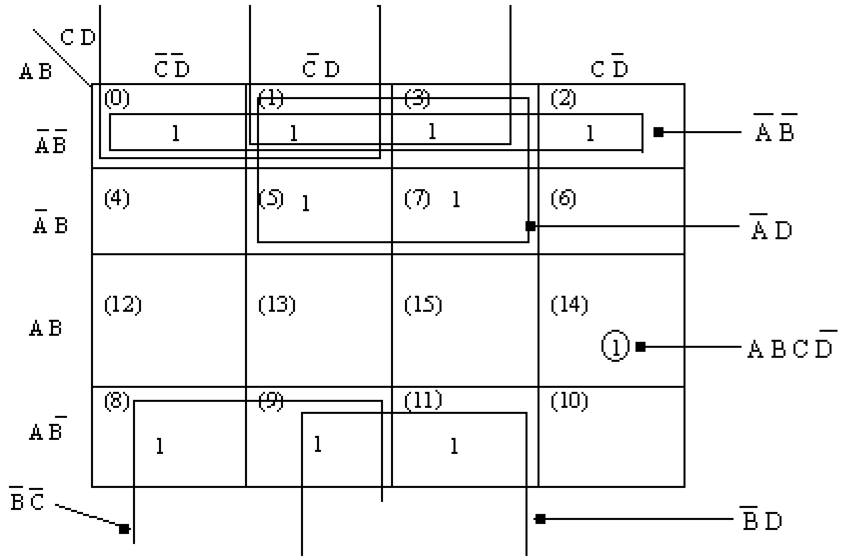


Fig. 4(a)

The simplified expression is $Y\,(A,B,C,D) = ABC\overline{D} + \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{B}D + \overline{A}D$

Fig.4 (b) shows the logic diagram for the simplified expression

$Y\,(A,B,\,C,\,D) = ABC\overline{D} + \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{B}D + \overline{A}D$

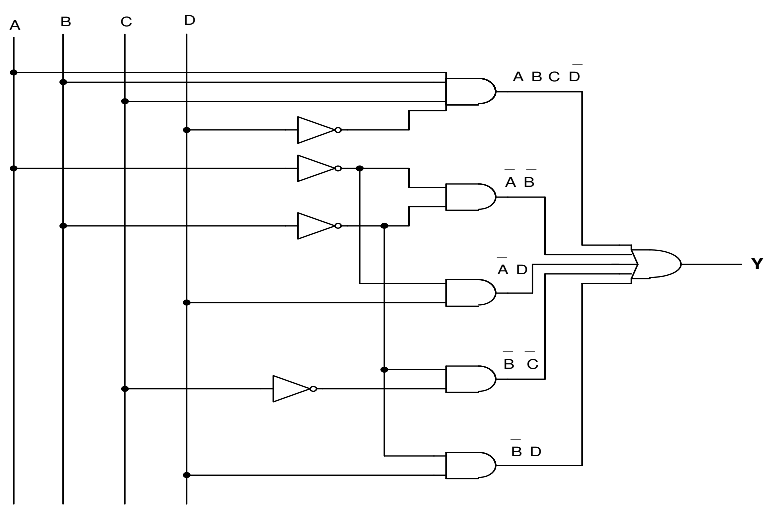


Fig.4(b) Logic diagram for Y

Q.13 Simplify the given expression to its Sum of Products (SOP) form. Draw the logic circuit for the simplified SOP function $Y = (A+B)(A+\overline{AB})C + \overline{A}(B+\overline{C}) + \overline{A}B + ABC$ **(5)**

Ans:

Simplification of given expression

$Y = (A + B)\,(A + \overline{AB}\,)\,C + \overline{A}\,(B + \overline{C}\,) + \overline{A}\,B + ABC$

in some of products (SOP) form:-

$$Y = (A + B)(A + \overline{AB})\,C + \overline{A}(B + \overline{C}) + \overline{A}B + ABC$$
$$=(A + B)(A + \overline{AB})\,C + \overline{A}(B + \overline{C}) + \overline{A}B + ABC$$
$$=(A + B)(A + \overline{A} + \overline{B})C + \overline{A}(B + \overline{C}) + \overline{A}B + ABC$$
$$=(A + B)(1 + \overline{B})C + \overline{A}(B + \overline{C}) + \overline{A}B + ABC \text{ (Because } A + \overline{A} = 1)$$
$$= (A + B)(C + \overline{B}C) + \overline{A}B + \overline{A}\,\overline{C} + \overline{A}B + ABC$$
$$= (A + B)(C + \overline{B}C) + \overline{A}B + \overline{A}\,\overline{C} + \overline{A}B + ABC$$
$$=AC + A\overline{B}C + BC + B\overline{B}C + \overline{A}B + \overline{A}\,\overline{C} + \overline{A}B + ABC$$
$$= AC + AC(\overline{B} + B) + BC + 0 + \overline{A}B + \overline{A}\,\overline{C} + \overline{A}B \text{ (Because } B\overline{B} = 0)$$
$$= AC + AC + BC + \overline{A}B + \overline{A}\,\overline{C} \text{ (Because } \overline{B} + B = 1)$$
$$= AC + BC + \overline{A}B + \overline{A}\,\overline{C} \text{ (Because } AC + AC = AC)$$
$$= C(A + B) + \overline{A}(B + \overline{C})$$

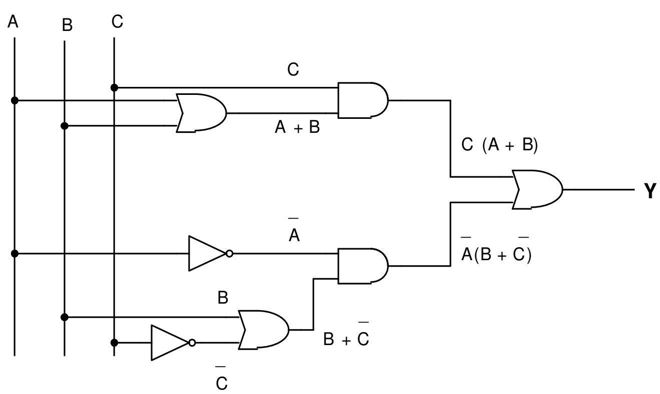


Fig.4(c) Simplified Logic Circuit

Q.14 Design a 8 to 1 multiplexer by using the four variable function given by $F(A,B,C,D) = \sum m(0,1,3,4,8,9,15)$. **(10)**

Ans:

<u>Design of 8 to 1 Multiplexer</u>: This is a four-variable function and therefore we need a multiplexer with three selection lines and eight inputs. We choose to apply variables *B,* C, and *D* to the selection lines. This is shown inTable 8.1. The first half of the minterms are associated with *A'* and the second half with *A*. By circling the minterms of the function and applying the rules for finding values for the multiplexer inputs, the implementation shown in Table.8.2.

The given function can be implemented with a 8-to-1 multiplexer as shown in fig.8(a). Three of the variables, B, C and D are applied to the selection lines in that order i.e., B is connected to s_2, C to s1 and D to s_0. The inputs of the multiplexer are 0, 1, A and A'. When BCD = 000,001 & 111 output F = 1 since I_0 & I_8 = 1 for BCD(000), I_1 = 1and I_9 =1 respectively. Therefore, minterms m_0 = A' B' C' m_1 = A' B' C, m_8 = A', B', C' and m_9 = A' B' C produce a 1 output. When BCD = 010, 101 and 110, output F = 0, since I_2, I_5 and I_6 respectively are equal to 0.

Minterm	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	1

Table .8.1 Truth Table for 8-1 Multiplexer

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\overline{A}$	(0)	(1)	2	(3)	(4)	5	6	7
A	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	$\overline{A}$	$\overline{A}$	0	0	A

Table 8.2 Implementation Table for 8 to 1 MUX

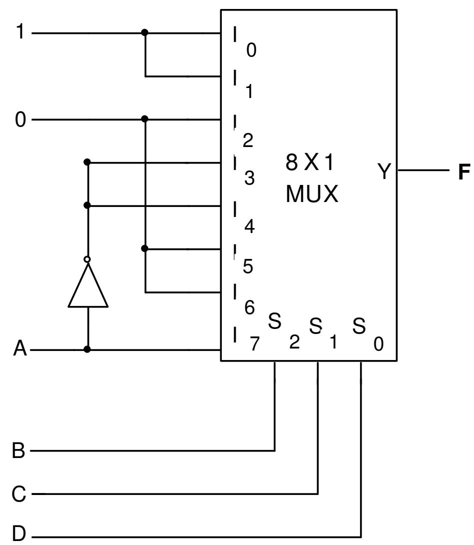


Fig.8(a) Logic circuit for 8-to-1 Multiplexer

Q.15 Convert the decimal number 82.67 to its binary, hexadecimal and octal equivalents. **(6)**

Ans:

(i)Conversion of Decimal number 82.67 to its Binary Equivalent

Considering the integer part 82 and finding its binary equivalent

2	82	
2	41	Remainder ----- 0 (LSB)
2	20	Remainder ----- 1
2	10	Remainder ----- 0
2	5	Remainder ------0
2	2	Remainder ----- 1
2	1	Remainder ---- 0
	0	Remainder ---- 1 (MSB)

The Binary equivalent is $(1010010)_2$

Now taking the fractional part i.e., 0.67

Fraction	Fraction X 2	Remainder New Fraction	Integer
0.67	1.34	0.34	1
0.34	0.68	0.68	0
0.68	1.36	0.36	1
0.36	0.72	0.72	0
0.72	1.44	0.44	1
0.44	0.88	0.88	0
0.88	1.76	0.76	1
0.76	1.52	0.52	1

It is seen that, it is not possible to get a zero as remainder even after 8 stages. The process continued further on an approximation can be made and the process is terminated here.

The binary equivalent is 0.10101011

Therefore, the binary equivalent of decimal number **82.67 is $(1010010.10101011)_2$**

(ii)Conversion of the binary equivalent of decimal number 82.67 into Hexadecimal:

The binary equivalent of decimal number 82.67 is $(1010010.10101011)_2$

Convert each 4-bit binary into an equivalent hexadecimal number i.e.

0101	0010	.1010	1011
5	2	A	B

Therefore, the hexadecimal equivalent of decimal number **82.67 is $(52.AB)_{16}$**

(iii)Conversioin of the binary equivalent of decimal number 82.67 into Octal number:

The binary equivalent of decimal number 82.67 is $(1010010.10101011)_2$

Convert each 3-bit binary into an equivalent octal number i.e.

001	010	010	.101	010	110
1	2	2	. 5	2	6

Therefore, the Octal equivalent of decimal number 82.67 is $(122.526)_8$

Q.16 Add 20 and (-15) using 2's complement. **(4)**

Ans:

Addition of 20 and (-15) using 2's Complement:

2	20	
2	10	Remainder ----- 0 (LSB)
2	5	Remainder ----- 0
2	2	Remainder ----- 1
2	1	Remainder ------0
	0	Remainder ----- 1(MSB)

2	16	
2	8	Remainder ----- 0 (LSB)
2	4	Remainder ----- 0
2	2	Remainder ----- 0
2	1	Remainder ------0
	0	Remainder ----- 1(MSB)

$(20)_{10}$ = 1 0 1 0 0

$(16)_{10}$ = 1 0 0 0 0

$(-16)_{10}$ = 0 1 1 1 1(1's Complement)
+1(2's Complement)

----
1 0 0 0 0

Therefore, 20 = 1 0 1 0 0
-16 = 1 0 0 0 0
----
1 0 0 1 0 0
↑
(Neglect)

Since the MSB of the sum is 0, which means **the result is positive i.e +4**

Q.17 Add 648 and 487 in BCD code. **(4)**

Ans:

Addition of 648 and 487 in BCD Code:

6 4 8 = 0 1 1 0 0 1 0 0 1 0 0 0
4 8 7 = 0 1 0 0 1 0 0 0 0 1 1 1
----
1 0 1 0 1 1 0 0 1 1 1 1

10 12 15

In the above problem all the three groups are invalid, because the four bit sum is more than 9. In such cases, add +6(i.e. 0110) to the four bit sum to skip the six invalid states. If a carry is generated when adding 6, add the carry to the next four bit group i.e.

```
 6 4 8 = 0110  0100  1000
 4 8 7 = 0100  1000  0111
 -------------------------------------------
            1010  1100  1111
          0110  0110  0110
       1   11   1  1   1   11
 ---------------------------------------------
    0001   0001  0011   0101
      ↓      ↓      ↓      ↓
    1      1      3      5
 ---------------------------------------------
```

Addition of 648 and 487 in BCD Code is 1135.

Q.18 Prove the following Boolean identities. **(4)**

(i) $XY + YZ + \bar{Y}Z = XY + Z$

(ii) $A.B + \overline{A}.B + \overline{A}.\overline{B} = \overline{A} + B$

Ans:

(i) Prove the Boolean Identity $XY + YZ + \bar{Y}Z = XY + Z$

L.H.S $= XY + YZ + \bar{Y}Z$

$= XY(Z+ \bar{Z}) + YZ + \bar{Y}Z\ (\because Z + \bar{Z} = 1)$

$= XYZ + XY\bar{Z} + YZ + \bar{Y}Z$

$= YZ(1+X) + XY\bar{Z} + \bar{Y}Z$

$= YZ + XY\bar{Z} + \bar{Y}Z\ \ (\because 1+X = 1)$

$= Z(Y+\bar{Y}) + XY\bar{Z}$

$= Z + XY\bar{Z}\ (\because Y+\bar{Y}=1)$

$= Z + XY (\because Z + XY\bar{Z} = Z + XY)$

= **R.H.S (Hence Proved)**

(ii) Prove the Boolean Identity $AB + \bar{A}B + \bar{A}\bar{B} = \bar{A} + B$

R.H.S $= \bar{A} + B$

$= \bar{A}(B + \bar{B}) + B(A + \bar{A})\ (\because B + \bar{B} = 1\ \&\ A + \bar{A} = 1)$

$= \bar{A}(B + \bar{B}) + B(A + \bar{A})$

$= \bar{A}B + \bar{A}\bar{B} + BA + B\bar{A}$

$= \bar{A}B + \bar{A}\bar{B} + BA\ (\bar{A}B + \bar{A}B = \bar{A}B)$

= **L.H.S (Hence Proved)**

Q.19 For $F = A.B.C + B.C.\overline{D} + \overline{A}.B.C$, write the truth table. Simplify using Karnaugh map and realize the function using NAND gates only. **(10)**

Ans:

Simplification of Logic Function $F = ABC + B\bar{C}D + \bar{A}BC$

(i)The Truth Table is given in Table 4.1

Inputs				Output (F)
A	B	C	D	
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 4.1

(ii) The Karnaugh Map is shown in fig.4(a).

The simplified expression is F = BC + BD

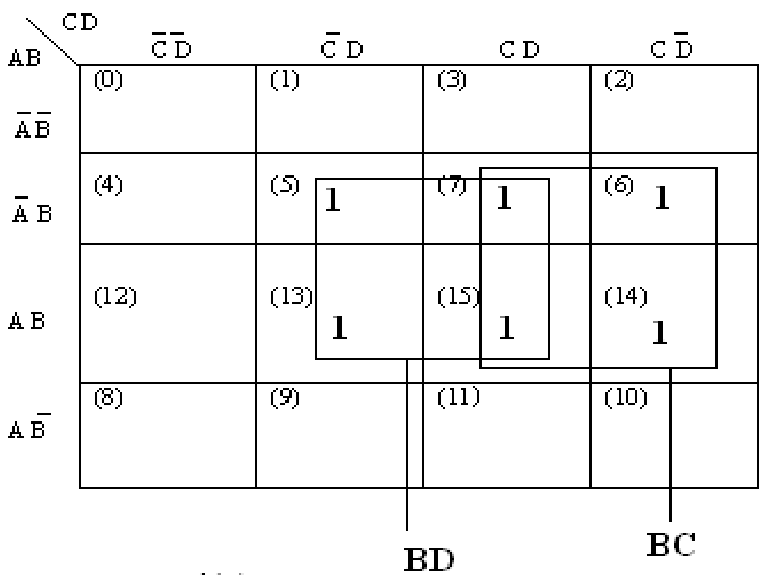


Fig.4(a)

(iii) The NAND-NAND Realization is shown in fig.4(b)

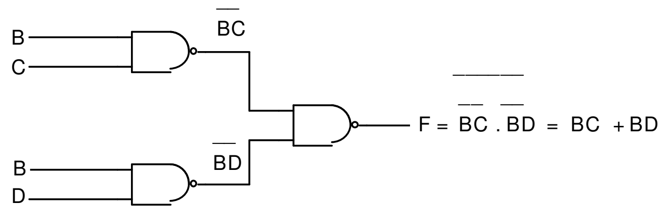


Fig. 4(b) NAND-NAND Realization

Q.20 Determine the analog output voltage of 6-bit DAC (R-2R ladder network) with V_{ref} as 5V when the digital input is 011100. **(10)**

Ans:

For 6-bit R-2R DAC ladder network, the output voltage is given by

$$V_0 = \frac{V_R}{2^n}\left(a_{n-1}2^{n-1} + a_{n-2}2^{n-2} + \cdots + a_1 2^1 + a_0 2^0\right)$$

Given Data : $V_R = 5V$, $n = 6$, $a_5=0$, $a_4=1$, $a_3=1$, $a_2=1$, $a_1=0$, $a_0=0$

$$V_0 = \frac{5}{2^6}\left(a_5 2^5 + a_4 2^4 + a_3 2^3 + a_2 2^2 + a_1 2^1 + a_0 2^0\right)$$

$$V_0 = \frac{5}{2^6}\left(0\times 2^5 + 1\times 2^4 + 1\times 2^3 + 1\times 2^2 + 0\times 2^1 + 0\times 2^0\right)$$

$$V_0 = 5\times\frac{28}{64} = \mathbf{2.1875\ V}$$

Q.21 Solve the following equations for X **(6)**

(i) $23.6_{10} = X_2$ (ii) $65.535_{10} = X_{16}$

Ans:

(i) Solve the equation $23.6_{10} = X_2$ for X

$23.6_{10} = X_2$

In order to find X, convert the Decimal number 23.6_{10} into its Binary form.

First take the decimal integer part 23 to convert into its equivalent binary form

2	23
2	11 ------- 1
2	5 --------1
2	2 --------1
2	1 --------0
	0 --------1

Hence $23_{10} = 10111_2$

Next take the decimal fractional part 0.6 to convert into its equivalent binary form.

Fraction	Fraction X 2	Remainder new fraction	Integer
0.6	1.2	0.2	1
0.2	0.4	0.4	0
0.4	0.8	0.8	0
0.8	1.6	0.6	1
0.6	1.2	0.2	1
0.2	0.4	0.4	0
0.4	0.8	0.8	0

It is seen that it is not possible to get a zero as remainder even after 7 stages. The process can be continued further or an approximation can be made and the process terminated here. The binary equivalent is 0.1001100.

Hence $\mathbf{23.6_{10} = 10111.1001100_2}$.

(ii) In order to find X, convert the Decimal number 65.535 into its equivalent Hexadecimal form. First taking the integer part 65 to convert into its equivalent Hexadecimal form.

16	65	
16	4	---- 1
	0	---- 4

Hence $65_{10} = 41_{16}$

Next take the decimal fractional part 0.6 to convert into its equivalent binary form.

Fraction	Fraction X 16	Remainder new fraction	Integer
0.535	8.56	0.56	8
0.56	8.96	0.96	8
0.96	15.36	0.36	15 (F)
0.36	5.76	0.76	5
0.76	12.16	0.16	12(C)
0.16	2.56	0.56	2
0.56	8.96	0.96	8

It is seen that it is not possible to get a zero as remainder even after 7 stages. The process can be continued further or an approximation can be made and the process terminated here. The Hexadecimal equivalent is 0.88F5C28.

Hence $\mathbf{65.535_{10} = 41.88F5C28_{16}}$.

Q.22 Perform the following additions using 2's complement **(5)**
(i) -20 to +26 (ii) +25 to -15

Ans:

(i) First convert the two numbers 20 and 26 into its 8-bit binary equivalent and find out the 2's complement of 20, then add -20 to +26.

20 = 0 0 0 1 0 1 0 0 (8-bit binary equivalent of 20)
$\overline{20}$ = 1 1 1 0 1 0 1 1 (1's complement)
+1

$\overline{20}$ = -20 = 1 1 1 0 1 1 0 0 (2's complement of 20)
+26 = 0 0 0 1 1 0 1 0 (8-bit binary equivalent of 26)

Addition of -20 to +26
= +6 = 0 0 0 0 0 1 1 0

Hence -20 to +26 = $(6)_{10}$ = $(0110)_{2.}$

(ii) First convert the two numbers 25 and 15 into its 8-bit binary equivalent and find out the 2's complement of 15, then add +25 to -15.

15 = 0 0 0 0 1 1 1 1 (8-bit binary equivalent of 15)
$\overline{15}$ = 1 1 1 1 0 0 0 0 (1's complement)
+1

$\overline{15}$ = -15 = 1 1 1 1 0 0 0 1 (2's complement of 15)
+25 = 0 0 0 1 1 0 0 1 (8-bit binary equivalent of 25)

Addition of -15 to +25
= +10 = 0 0 0 0 1 0 1 0

Hence -15 to +25 = $(10)_{10}$ = $(1010)_{2.}$

Q.23 (i) Convert the decimal number 430 to Excess-3 code: **(6)**
(ii) Convert the binary number 10110 to Gray code:

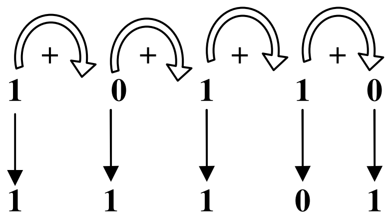
Ans:

(i) Excess 3 is a digital code obtained by adding 3 to each decimal digit and then converting the result to four bit binary. It is an unweighted code i.e., no weights can be assigned to any of the four digit positions.

4	3	0
+ 3	+ 3	+ 3
7	6	3
↓	↓	↓
0111	0110	0011 (Excess-3 Code)

(ii) The rules for changing binary number 10110 into its equivalent Gray code are, the left most bit (MSB) in Gray code i.e., 1 is the same as the left most bit in binary and

add the left most bit (1) to the adjacent bit (0) then add the next adjacent pair and discard the carry. Continue this process till completion.



Hence Gray equivalent of Binary number 10110 is 11101.

Q.24 Verify that the following operations are commutative but not associative **(6)**
(i) NAND (ii) NOR

Ans:

(i) Commutative Law is $\overline{AB} = \overline{BA}$. To verify whether the NAND operation is Commutative or not, prepare truth table shown in Table No.3.1

A	B	$\overline{AB}$	$\overline{BA}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Table No.3.1

From the Table No.3.1, we observe that the last two columns are identical, which means

$$\overline{AB} = \overline{BA}$$

Associative Law is $\overline{A.\overline{(B.C)}} = \overline{\overline{(A.B)}.C}$

To verify whether the NAND operation is Associative or not, prepare truth table shown in Table No.3.2

A	B	C	$\overline{A.\overline{(B.C)}}$	$\overline{\overline{(A.B)}.C}$
0	0	0	1	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

Table No.3.2

From the Table No.3.2, we observe that the last two columns are not identical, which means

$$\overline{A.\overline{(B.C)}} \neq \overline{\overline{(A.B)}.C}$$

(ii) Commutative Law is $\overline{A+B} = \overline{B+A}$. To verify whether the NOR operation is Commutative or not, prepare truth table shown in Table No.3.3

A	B	$\overline{A+B}$	$\overline{B+A}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

Table No.3.3

From the Table No.3.3, we observe that the last two columns are identical, which means

$$\overline{A+B} = \overline{B+A}$$

Associative Law is $\overline{A+\overline{(B+C)}} = \overline{\overline{(A+B)}+C}$

To verify whether the NOR operation is Associative or not, prepare truth table shown in Table No.3.4

A	B	C	$\overline{A+\overline{(B+C)}}$	$\overline{\overline{(A+B)}+C}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	1
1	1	1	0	0

Table No.3.4

From the Table No.3.4, we observe that the last two columns are not identical, which means

$$\overline{A.+\overline{(B+C)}} \neq \overline{\overline{(A+B)}+C}$$

Q.25 Prove the following equations using the Boolean algebraic theorems: **(5)**

(i) A + $\bar{A}$.B + A . $\bar{B}$ = A + B (ii) $\bar{A}$BC + A$\bar{B}$C + AB$\bar{C}$ + ABC = AB + BC + AC

Ans:

(i) Given equation is A + $\bar{A}$.B + A.$\bar{B}$ = A + B

L.H.S. = A + $\bar{A}$.B + A.$\bar{B}$

= (A + A.$\bar{B}$) + $\bar{A}$.B

= A (1+$\bar{B}$) + $\bar{A}$.B

= A + $\bar{A}$.B (∵ 1+$\bar{B}$ =1)

= (A + $\bar{A}$) (A + B)

= (A + B) (∵ A + $\bar{A}$ = 1)

= **R.H.S**

Hence Proved

(ii) Given equation is $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC = AB + BC + AC$

L.H.S = $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$

$= \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$

$= \overline{A}BC + A\overline{B}C + AB(C + \overline{C})$

$= \overline{A}BC + A\overline{B}C + AB \ (\because C + \overline{C} = 1)$

$= \overline{A}BC + A(B + \overline{B}C)$

$= \overline{A}BC + A(B + C) \ (\because B + \overline{B}C = B + C)$

$= \overline{A}BC + A\,B + AC$

$= C(A + \overline{A}B) + A\,B + AC$

$= C(A + B) + A\,B + AC \ (\because A + \overline{A}B = A + B)$

$= AC + BC + AB + AC$

$= AB + BC + AC \ (\because AC + AC = AC)$

= **R.H.S**

Hence Proved

Q.26 A staircase light is controlled by two switches one at the top of the stairs and another at the bottom of stairs **(5)**

(i) Make a truth table for this system.

(ii) Write the logic equation is SOP form.

(iii) Realize the circuit using AND-OR gates.

Ans:

A staircase light is controlled by two switches S_1 and S_2, one at the top of the stairs and another at the bottom of the stairs. The circuit diagram of the system is shown in fig.4(a).

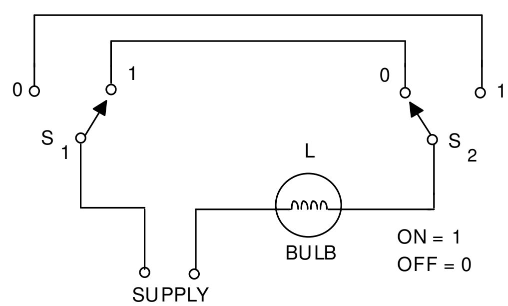


Fig.4(a) Circuit diagram

(i) The truth table for the system is given in truth table 4.1

S_1	S_2	L
0	0	0
0	1	1
1	0	1
1	1	0

Table 4.1

(ii) The logic equation for the system is given by $L = \overline{S_1}\,S_2 + S_1\,\overline{S_2}$

(iii) Realization of the circuit using AND-OR gates is shown in fig 4(b)

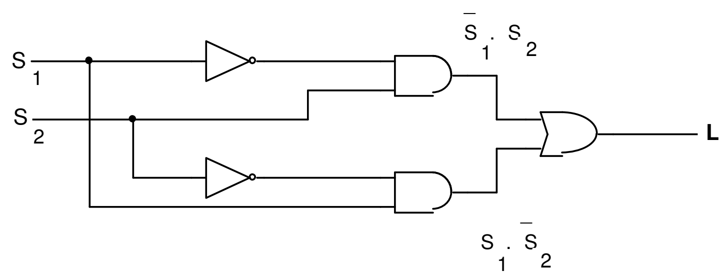


Fig.4(b) Logic Diagram for the system

Q.27 Minimize the following logic function using K-maps and realize using NAND and NOR gates.
$F(A,B,C,D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$ **(9)**

Ans:

Minimization of the logic function F(A, B, C, D) = ∑ m(1,3,5,8,9,11.15) + d(2,13) using K-maps and Realization using NAND and NOR Gates

(i) Karnaugh Map for the logic function is given in table 4.1

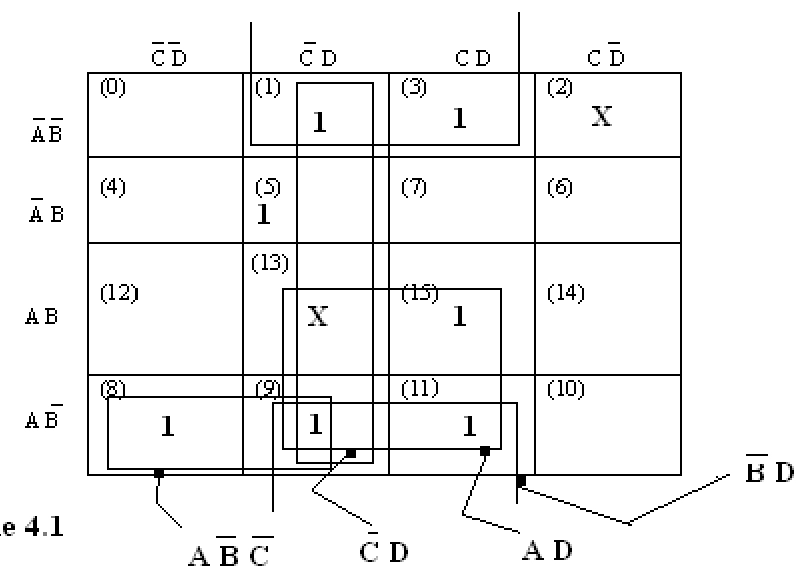


Table 4.1

The minimized logic expression in SOP form is $F = A\bar{B}\bar{C} + \bar{C}D + \bar{B}D + AD$

The minimized logic expression in POS form is $F = (A + \bar{B} + \bar{C})(\bar{C} + D)(\bar{B} + D)(A + D)$

(ii) Realization of the expression using NAND gates:

The minimized logic expression in SOP form is $F = A\bar{B}\bar{C} + \bar{C}D + \bar{B}D + AD$ and the logic diagram for the simplified expression is given in fig.4(c)

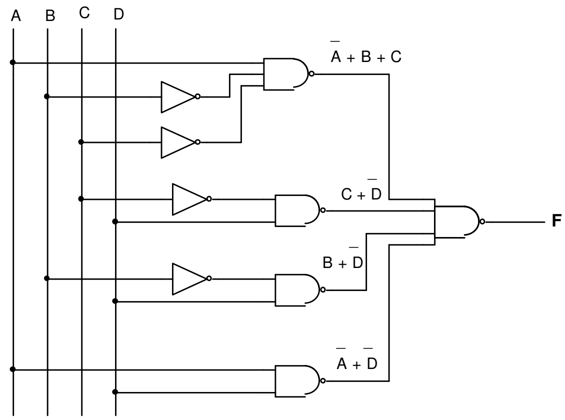


Fig.4(c) Logic Diagram

(iii) Realization of the expression using NOR gates:

The minimized logic expression in POS form is $F = (A + \overline{B} + \overline{C})\,(\overline{C} + D)\,(\overline{B} + D)\,(A + D)$ and the logic diagram for the simplified expression is given in fig.4(d)

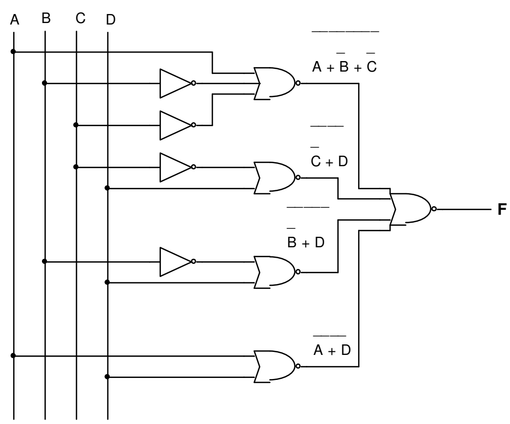


Fig.4(d) Logic Diagram

Q.28 Design a 4 to 1 Multiplexer by using the three variable function given by $F(A,B,C) = \sum m(1,3,5,6)$ **(7)**

Ans:

Design of 4 to 1 Multiplexer by using the three variable function given by $F(A,B,C) = \sum m(1,3,5,6)$

The function **$F(A,B,C) = \sum m(1,3,5,6)$** can be implemented with a 4-to-1 multiplexer as shown in Fig.7(a). Two of the variables, B and C are applied to the selection lines in that order, i.e., B is connected to S_1 and C to S_0. The inputs of the multiplexer are 0, I, A, and A'.

When $BC = 00$, output $F = 0$ since $I_0 = 0$. Therefore, both minterms $m_0 = A'B'C'$ and $m4 = AB'C'$ produce a 0 output, since the output is 0 when $BC = 00$ regardless of the value of A.

When $BC = 01$, output $F = 1$, since $I_1 = 1$. Therefore, both minterms $m_1 = A'B'C$ and

$m_5 = AB'C$ produce a 1 output, since the output is 1. when $BC = 01$ regardless of the value of A.

When $BC = 10$, input I_2 is selected. Since A is connected to this input, the output will be equal to 1 only for minterm $m_6 = ABC'$, but not for minterm $m_2 = A'BC'$, because when $A' = I$, then $A = 0$, and since $I_2 = 0$, we have $F = 0$.

Finally, when $BC = 11$, input I_3 is selected. Since A' is connected to this input, the output will be equal to 1 only for minterm $m_3 = A'BC$, but not for $m_7 = ABC$. This is given in the Truth Table shown in Table No 7.1

Minterm	A	B	C	F
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

Table 7.1 Truth Table

	I_0	I_1	I_2	I_3
A`	0	(1)	2	(3)
A	4	(5)	(6)	7
	0	1	A	A`

Fig.7(a) Implementation Table

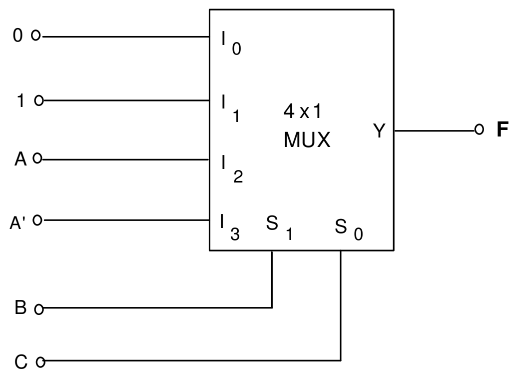


Fig.7(b) Logic Diagram of 4X1 Multiplexer

Q.29 Find the conversion time of a Successive Approximation A/D converter which uses a 2 MHz clock and a 5-bit binary ladder containing 8V reference. What is the Conversion Rate? **(4)**

Ans:

Given data:

Frequency of the clock (F) = 2 MHZ

Number of bits (n) = 5

(i) Conversion Time (T) = $\frac{n}{clockrate} = \frac{5}{2X10^6} = 2.5\ \mu\text{sec}$

(ii) Conversion Rate = $\frac{1}{T} = \frac{1}{2.5X10^{-6}}$ = 400,000 conversions/sec

Q.30 A 6-bit R-2R ladder D/A converter has a reference voltage of 6.5V. It meets standard linearity. Find

(i) The Resolution in Percent.

(ii) The output voltage for the word 011100. **(4)**

Ans:

Given Data Number of Bits (n) = 6

Reference Voltage (V_R) = 6.5 V

For R-2R Ladder D/A Converter,

(i)The Resolution in Percent is given by $\frac{1}{2^n-1} = \frac{1}{2^6-1} = \frac{1}{63} = 1.59\ \%$

(ii)The Output Voltage (V_O) of 6-bit R-2R Ladder D/A Converter for the word 011100 is given by

$$V_O = \frac{V_R}{2^n}\left[a_{n-1}.2^{n-1} + a_{n-2}.2^{n-2} + ----+a_1 2^1 + a_0 2^0\right]$$

$$V_O = \frac{6.5}{2^6}\left[0.2^{6-1} + 1X\,2^{5-1} + 1X\,2^{4-1} + 1X\,2^{3-1} + 0X\,2^{2-1} + 0X\,2^{0}\right]$$

$$V_O = \frac{6.5}{2_6}\left[2^4 + 2^3 + 2^2\right]$$

$$V_O = 2.84\text{ V.}$$

Q.31 Convert 2222 in Hexadecimal number. **(4)**

Ans:

	2222	
16	138	14
16	8	10
	0	8

↑ =8AE

Q.32 Subtract –27 from 68 using 2's complements. **(6)**

Ans:

68-(-27)=68-(-27)using 2's complement
2's complement representation of 68=01000100(64+4)
2's complement representation of - (-27) = 00011011 =+ 27
11100101 =-27 in 2's complement
Now add 68 and 27

68	0 1 0 0 0 1 0 0
-(-27)	+ 0 0 0 1 1 0 1 1
95	0 1 0 1 1 1 1 1 1

Which is equal to +95

Q.33 Divide $(101110)_2$ by $(101)_2$. **(4)**

Ans:

```
101 | 1 0 1 1 1 0 | 1 0 0 1
      1 0 1
      -----------
      0 0 0 1 1 0
            1 0 1
            -----
            0 0 1
```

Quotient -1001
Remainder -001

Q.34 Prove the following identities using Boolean algebra:

(i) $(A+B)(A+\overline{AB})C + \overline{A}(B+\overline{C}) + \overline{A}B + ABC = C(A+B) + \overline{A}(B+\overline{C})$.

(ii) $\overline{\overline{A\overline{(A\cdot B)}}\cdot\overline{B\overline{(A\cdot B)}}} = A \oplus B$.

(iii) $\overline{\overline{AB} + \overline{A} + AB} = 0$. **(9)**

Ans:

(i) (A+B)(A+A'B')C+A'(B+C')+A'B+ABC

=C(A+B)+A'(B+C')

LHS (A+B)(A+A'+B')C+A'B+A'C'+A'B+ABC

= (A+B)(1+B')C+A'B+ A'C'+ABC as (A+A'=1)

= (A+B).1.C+A'B+ A'C'+ABC

= AB+AC+A'B+ A'C'+ABC

= ABC+AB+ABC+AC+A'B+A'C'

AB(C+1)+AC(B+1) +A'B+ A'C'

= AB+AC+A'B+ A'C'

= C(A+B) + A'(B+C') = **RHS**

Hence Proved

(ii) $\overline{\overline{A(\overline{A.B})}.\overline{B(\overline{A.B})}} = A \oplus B$

Let us take $X = \overline{A(\overline{A.B})}$

$Y = \overline{B(\overline{A.B})}$

So we have $\overline{X.Y} = A \oplus B$ -------3

Also $X = \overline{A(\overline{A.B})}$

$= \overline{A(A' + B')}$

By using DeMorgan's Law (AB)'=A'+B'

X = (A(A'+B'))'=(AA'+AB')'=(AB')'=(A'+B) ------1

Now Y = (B(AB)')'=[B(A'+B')]'= [A'B+BB']'=(A'B)'=(A+B') ------2

Now Combining X & Y from 1 & 2 above, we have L.H.S in 3 as :

((A+B')(A'+B))'

=[AA'+BB+A'B'+AB]'

=(AB+A'B')'

=A XOR B = **RHS**

Hence Proved

(iii) ((AB)'+A'+AB)'=0

LHS $\overline{(\overline{AB} + \overline{A} + AB)}$

$= (1 + A')'$ since $\overline{AB} + AB = 1$

$= 1'$ since $1 + A' = 1$

= 0 **= RHS Hence Proved**

Q.35 A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations

A is False, B is True

A is False, C is True

A, B, C are False

A, B, C are True

(i) Write the Truth table for F. Use the convention True=1 and False = 0.
(ii) Write the simplified expression for F in SOP form.
(iii) Write the simplified expression for F in POS form.
(iv) Draw logic circuit using minimum number of 2-input NAND gates. **(7)**

Ans:

(i) Making the truth table

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

A is false b is true → For both value of c F is true.

(ii) Simplified expression for F can be found by K-map

A/BC	00	01	11	10
0	1	1	1	1
1	0	0	1	0

In SOP Form

F = A'+BC

(iii) Simplified expression for F in POS form

I. In POS Form MINIMIZE ZEROS

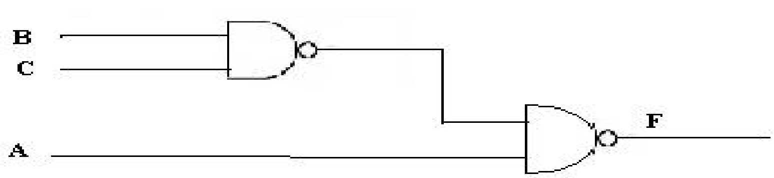
F'=AB'+AC'

II. F=A'+BC taking complement twice

F'=(A'+BC)'=(A.(BC)')

F"=F=(A.(BC)')'

(iv) Logic circuit by using minimum number of 2-input NAND gates



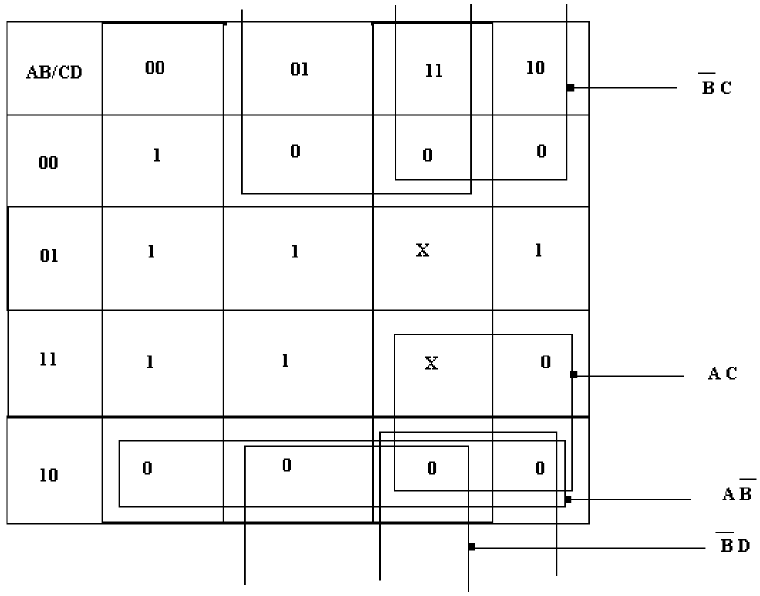
Q.36 Minimise the logic function

$F(A,B,C,D)=\Pi M(1,2,3,8,9,10,11,14)\cdot d(7,15)$

Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only. **(7)**

Ans:

F=∏M(1,2,3,8,9,10,11,14).d(7, 15)



F'=B'D+B'C+AC+AB'

By Complementing F

F=(B'D+B'C+AC+AB')'

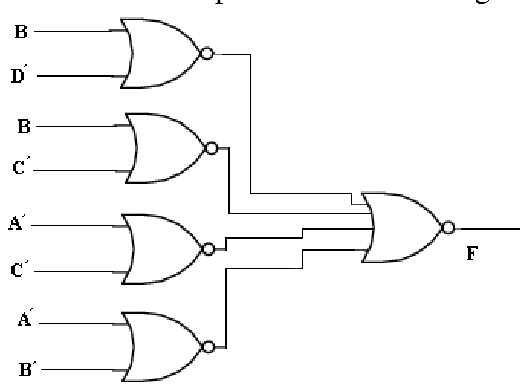
= [(B'D)'(B'C)'(AC)'(AB')']'

= (B+D')(B+C')(A'+C')(A'+B)

Taking complement twice and without opening the bracket

F=[(B+D')+(B+C')'('A'+C')+(A'+B)]'

The logic circuit for the simplified function using NOR gates



Q.37 The capacity of 2K × 16 PROM is to be expanded to 16 K × 16. Find the number of PROM chips required and the number of address lines in the expanded memory. **(4)**

Ans:

Required capacity =16k x 16

Available chip (PROM) =2k x 16

The no of chip $= \frac{16k \times 16}{2k \times 16} = 8$

In the chip total word capacity = 2×2^{10}

Thus the address line required for the single chip = 11
In the expanded memory the word capacity 16k = 2^{14}
Now the address lines required are 14. Among then 11 will be common and 3 will be connected to 3 x8 decoder.

Q.38 Perform following subtraction
(i) 11001-10110 using 1's complement
(ii) 11011-11001 using 2's complement **(8)**

Ans:
(**i**) 11001 - 10110
1' s Compliment of 10110 = 01001

```
  1 1 0 0 1
+ 0 1 0 0 1
-----------------
 1 0 0 0 1 0
```

Add 1 and ignore carry.
Ans is 00011 = 3.

(ii) 11011 – 11001 = A – B
2's complement of B = 00111

```
   1 1 0 1 1
 + 0 0 1 1 1
 1 0 0 0 1 0
```

Ignore carry to get answer as 00010 = 2.

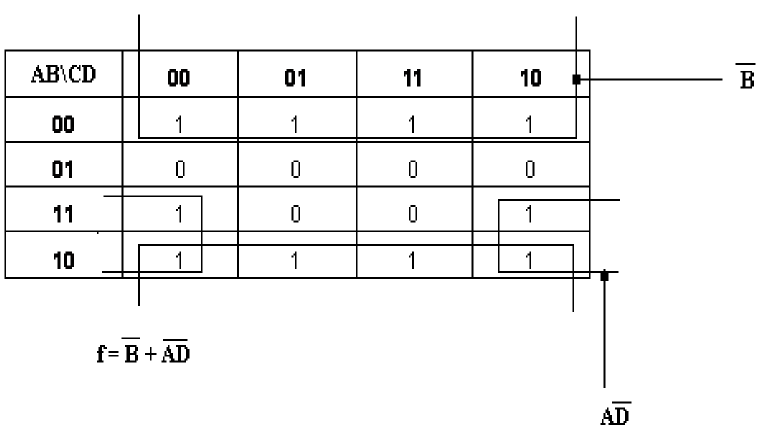
Q.39 Reduce the following equation using k-map

$$Y = \bar{A}\bar{B}\bar{C} + A\bar{C}\bar{D} + A\bar{B} + ABC\bar{D} + \bar{A}\bar{B}C$$ **(8)**

Ans:

$$Y = \bar{A}\bar{B}\bar{C} + A\bar{C}\bar{D} + A\bar{B} + \bar{A}\bar{B}C$$

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + A\bar{B}CD + A\bar{B}\bar{C}D$$
$$+ A\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + ABC\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD$$



Q.40 Write the expression for Boolean function

F (A, B, C) = $\sum$m (1,4,5,6,7) in standard POS form. **(8)**

Ans:

$f(A,B,C) = \Sigma M(1,4,5,6,7)$ in standard POS form

$F = m_1 + m_4 + m_5 + m_6 + m_7$

$F = \Sigma m(1,4,5,6,7)$

$= \prod M(0,2,3)$

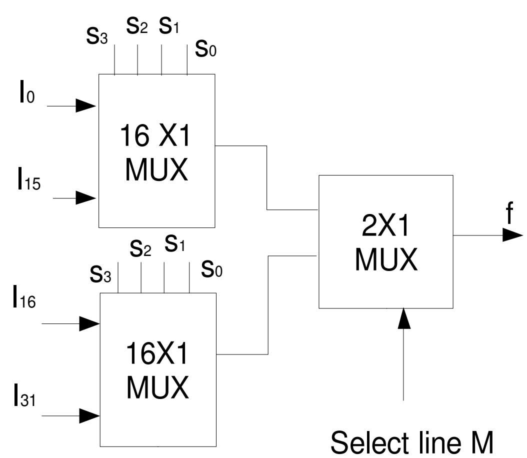
$= M_0 M_2 M_3$

$= (A+B+C)(A+\overline{B}+C)(A+\overline{B}+\overline{C})$

Q.41 Design a 32:1 multiplexer using two 16:1 multiplexers and a 2:1 multiplexer. **(8)**

Ans:

To design a 32 X 1 MUX using



Two 16 X 1 MUX & one 2 X 1

There are total 32 input lines and one O/P line. The 2 X 1 MUX will transmit one of the two I/P to output depending upon its select line M. For M = 0 upper MUX (I_0 – I_{15}) will be selected and M = 1 lower MUX (I_{16} – I_{31}) will be selected.

Q.42 Implement the following function using a 3 line to 8 line decoder.

S (A,B,C) = $\sum$ m(1,2,4,7)

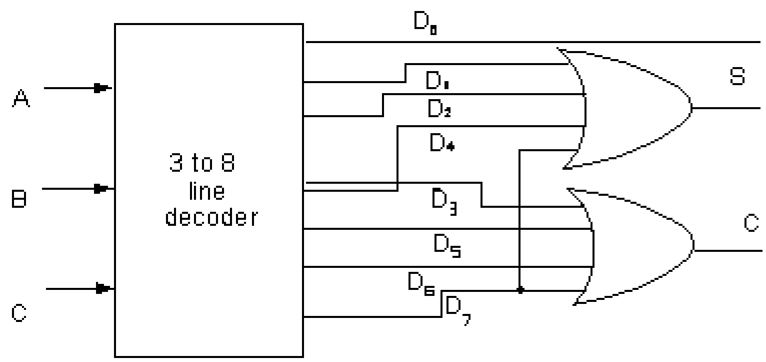
C (A,B,C) = $\sum$ m (3,5,6,7) **(8)**

Ans:

S (A,B,C) = m (1,2,4,7)

C (A,B,C) = m (3,5,6,7)

These are full adder's output as sum (S) and carry (C). We know that 3 to 8 line decoder generates all the minterms from 0 to 7. In the decoder shown in the figure, Do correspond to minterm m_o, and so on. So by ORing appropriate outputs of the decoder we can implement these functions.



Q.43 Perform the following operations using the 2's complement method:
(i) 23 – 48 (ii) – 48 – 23 **(4)**

Ans:

(i) 23 - 48

add them

23	0 1 0 1 1 1
- (- 48)	+ 0 1 0 0 0 0
71	1 0 0 1 1 1

(ii) – 48 - 23 = - 48 + (-23)

-48 = 1 1 0 1 0 0 0 0

-23 = 1 1 1 0 1 0 0 1

1 1 0 1 1 1 0 0 1 = -71

↓

Carry is discarded

Q.44 Prove the following Boolean identities using the laws of Boolean algebra:

(i) $(A+B)(A+C) = A+BC$

(ii) $ABC + A\overline{B}C + AB\overline{C} = A(B+C)$ **(4)**

Ans:

(i) (A+B)(A+C)=A+BC

LHS AA+AC+AB+BC=A+AC+AB+BC

OR A((C+1)+A(B+1))+BC

OR A+A+BC

OR A+BC = **RHS**

Hence Proved

(ii) ABC+AB'C+ABC'=A(B + C)

LHS AC(B+B')+AB(C+C')

OR AC+AB

OR A(B+C)= **RHS**

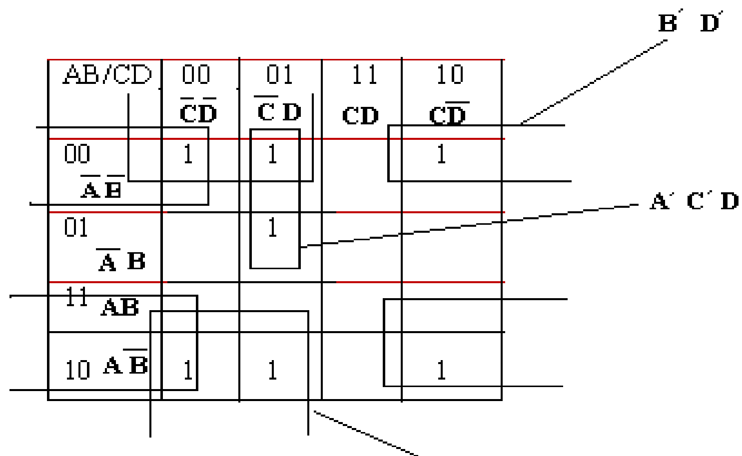
Hence Proved

Q.45 The Karnaugh map for a SOP function is given below in Fig.1. Determine the simplified SOP Boolean expression. **(5)**

AB \ CD	00	01	11	10
00	1	1		1
01		1		
11				
10	1	1		1

Fig.1

Ans:



$F = B'C' + A'C'D + B'D'$

Q.46 A certain memory has a capacity of 4K×8
(i) How many data input and data output lines does it have?
(ii) How many address lines does it have?
(iii) What is its capacity in bytes? **(5)**

Ans:
(i) available capacity =4Kx8
$= 2^{10} \times 2^{10} \times 8$
$= 2^{12} \times 8$

As in the 4Kx8 ,the second number represents the number of bits in each word so the number of data input lines will be 8(also the data output lines) .

(ii) It has total 4K (2^{12}) address line which are required to address 2^{12} locations.

(iii) Its capacity in bytes is 4K bytes.

Q.47 A 5-bit DAC produces an output voltage of 0.2V for a digital input of 00001. Find the value of the output voltage for an input of 11111. What is the resolution of this DAC? **(6)**

Ans:
For the Digital output of 00001
Output voltage is =0.2 volt =Resolution
The output=.2x31=15.5volts
Resolution=(0.2volt)/(15.5v)x100=1.290

Q.48 An 8-bit successive approximation ADC has a resolution of 20mV. What will be its digital output for an analog input of 2.17V? **(4)**

Ans:

Resolution =20mv
Analog input =2.17v
Equivalent value=(2.17)/(2.17)=108.5
Equivalent Binary value=1101100.1

Q.49 A microprocessor uses RAM chips of 1024×1 capacity.

(i) How many chips will be required and how many address lines will be connected to provide capacity of 1024 bytes.
(ii) How many chips will be required to obtain a memory of capacity of 16 K bytes. **(5)**

Ans:
(i) Available chips = 1024 x 1 capacity
Required capacity = 1024 x 8 capacity

$$No.\ of\ Chips = \frac{1024X8}{1024X1} = 8$$

Number of address lines are required = 10 (i.e. 1024 = 2^{10})
As the word capacity is same (1024) so same address lines will be connected to all chips.

(ii)

$$No.\ Of\ Chips\ Required = \frac{16X1024X8}{1024X1} = 128$$

Q.50 Find the Boolean expression for logic circuit shown in Fig.1 below and reduce it using Boolean algebra. **(6)**

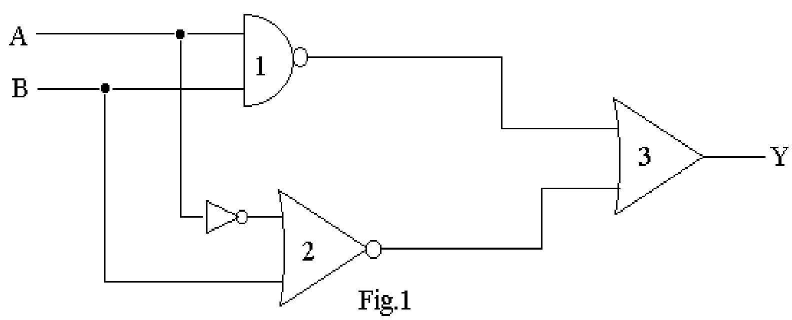


Fig.1

Ans:

Y = (AB)' + (A' + B)'
= A' + B' + AB' Using Demorgan's Theorem.
= A' + B'(1+A)
= A' + B' Since 1+A=1

Q.51 Implement the following function using 4-to-1 multiplexer.

$$Y(A,B,C) = \sum (2,3,5,6)$$ **(8)**

Ans:

Y(A,B,C)=∑(2,3,5,6)

Let us take B,C as the select bits and A as input. To decide the input we write.

Y = A'BC'+A'BC+AB'C+ABC'

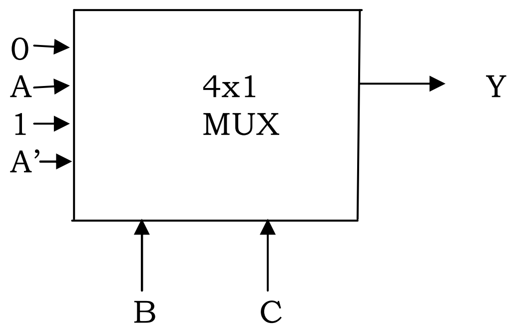
= 0 if B=0, C=0

= A if B=0, C=1

= 1 if B=1, C=0

= A' if B=1, C=1

The corresponding implementation is shown in the figure. Thus



Q.52 Design a mod-12 Synchronous up counter. **(8)**

Ans:

Design a mod 12 synchronous counter using D-flipflops.

I state table

Present state | Next state | Required D Inputs

A	B	C	D	A	B	C	D	D_A	D_B	D_C	D_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	0	1	0	0	0	1	0	0

First draw the state table having present state, next state and required flip-flop input to give the transition. D flip flop gives the output same as the next state itself. Then solve by using K maps to find out D_A D_B D_C D_D for all states.

Unused states are 1100,1101,1110,1111 they can be treated as don't care conditions from the table. Draw Karnaugh-maps for D_A, D_B, D_C and D_D as follows and obtain Boolean expressions for them.

AB/ CD	00 $\bar{C}\bar{D}$	01 $\bar{C}D$	11 CD	10 $C\bar{D}$
00 $\bar{A}\bar{B}$	0	0	0	0
01 $\bar{A}B$	0	0	1	0
11 AB	X	X	X	X
10 $A\bar{B}$	1	1	0	1

Groups: BCD, AC′, AD′

$$D_A = BCD + AC' + AD'$$

AB/ CD	00 $\bar{C}\bar{D}$	01 $\bar{C}D$	11 CD	10 $C\bar{D}$
00 $\bar{A}\bar{B}$	0	0	1	0
01 $\bar{A}B$	1	1	0	1
11 AB	X	X	X	X
10 $A\bar{B}$	0	0	0	0

Groups: A′B′CD, BC′, BD′

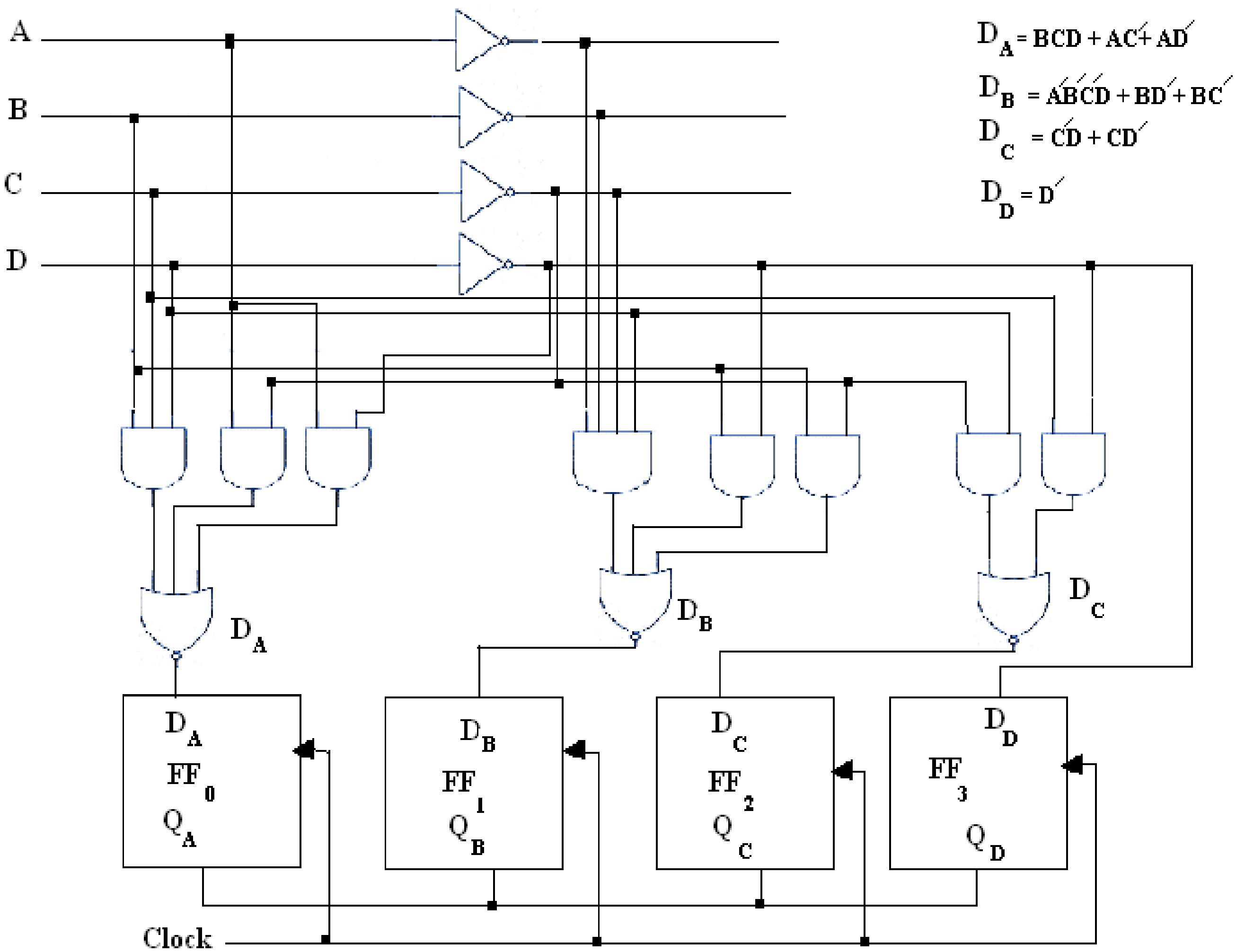
$$D_B = A'B'CD + BD' + BC'$$

AB/ CD	00 $\bar{C}\bar{D}$	01 $\bar{C}D$	11 CD	10 $C\bar{D}$
00 $\bar{A}\bar{B}$	0	1	0	1
01 $\bar{A}B$	0	1	0	1
11 AB	X	X	X	X
10 $A\bar{B}$	0	1	0	1

$$D_C = \bar{C}D + C\bar{D}$$

AB/ CD	00 $\bar{C}\bar{D}$	01 $\bar{C}D$	11 CD	10 $C\bar{D}$
00 $\bar{A}\bar{B}$	1	0	0	1
01 $\bar{A}B$	1	0	0	1
11 AB	X	X	X	X
10 $A\bar{B}$	1	0	0	1

$$D_D = \bar{D}$$



Logic diagram for mod-12 Synchronous up-counter

Q.53 Find how many bits of ADC are required to get an resolution of 0.5 mV if the maximum full scale voltage is 10 V. **(8)**

Ans:

Resolution=.5mv

Full scale output=+10v

%resolution =(5mv)/10x100=0.05%

No of bits =Log_2(2x1000) = 20

Q.54 Convert the decimal number 45678 to its hexadecimal equivalent number. **(4)**

Ans:

$(45678)_{10}=(B26E)_{16}$

16	45678		
16	2854	14	→ E
16	178	6	→ 6
16	11	2	→ 2
	0	11	→ B

$(45678)_{10}=(B26E)_{16}$

Q.55 Write the truth table of NOR gate. **(4)**

Ans:

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

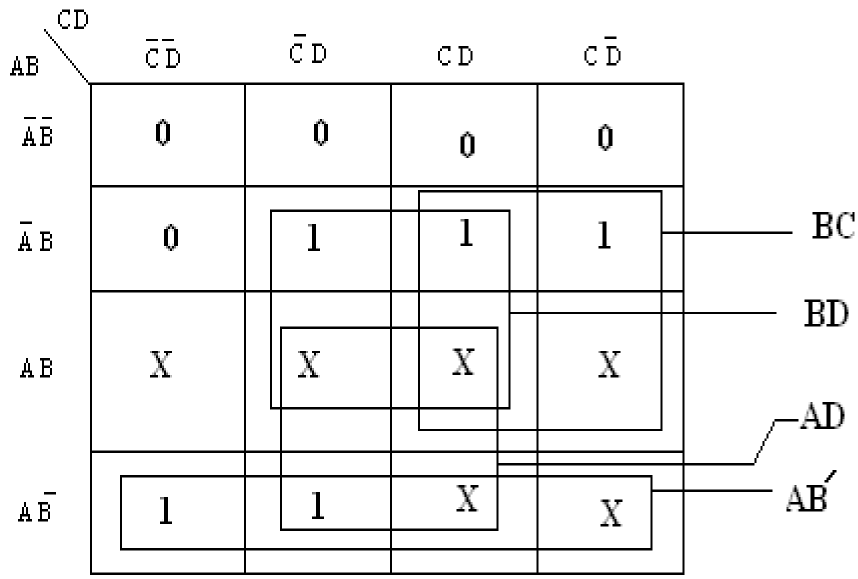
Q.56 Design a BCD to excess 3 code converter using minimum number of NAND gates. Hint: use k map techniques. **(8)**

Ans:

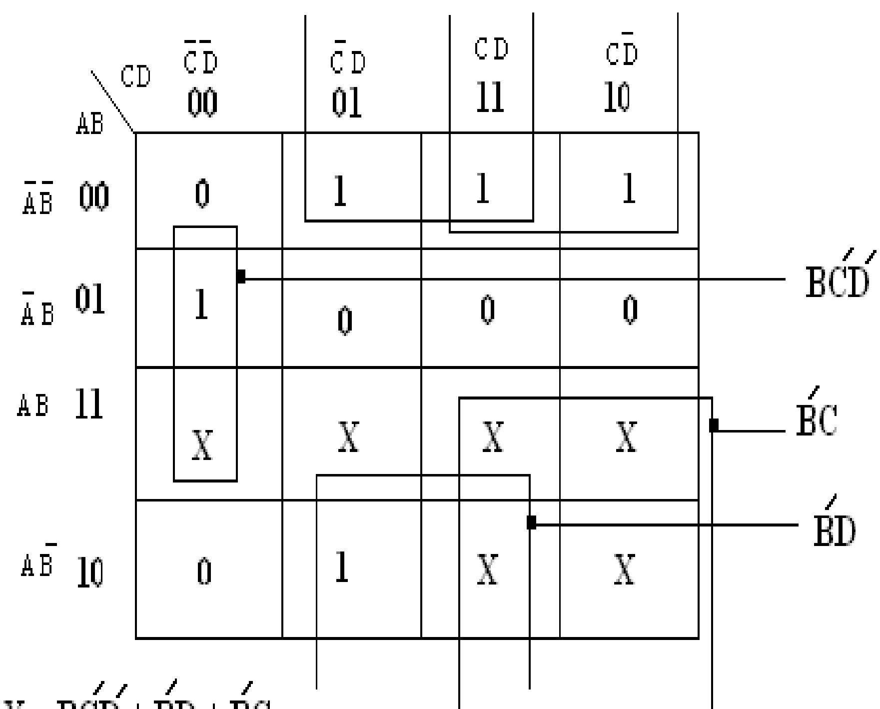
First we make the truth table

BCD no A B C D	EXCESS-3 NO W X Y Z
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	0 1 1 1
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0

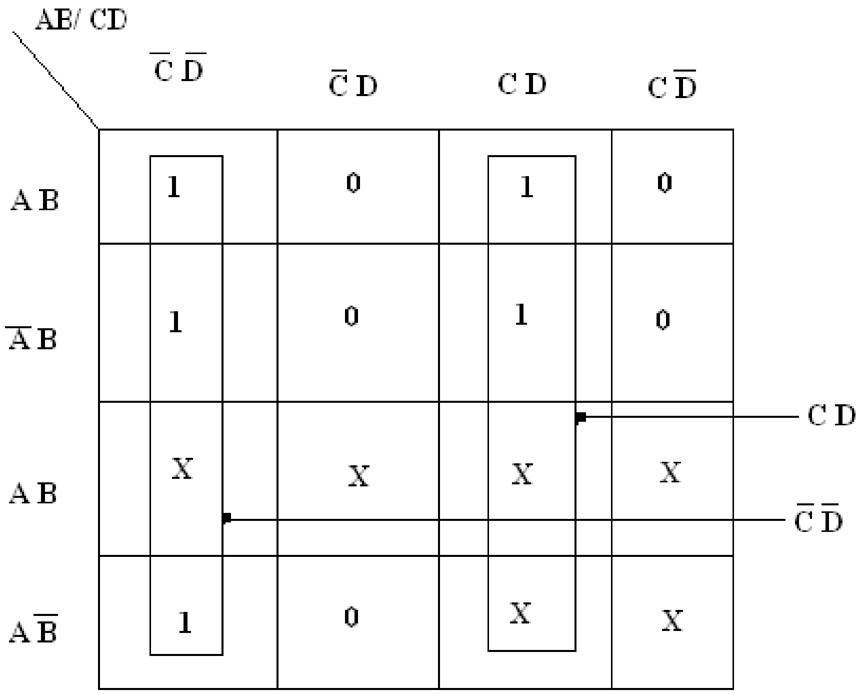
Then by using K maps we can have simplified functions for w, x, y, z as shown below:



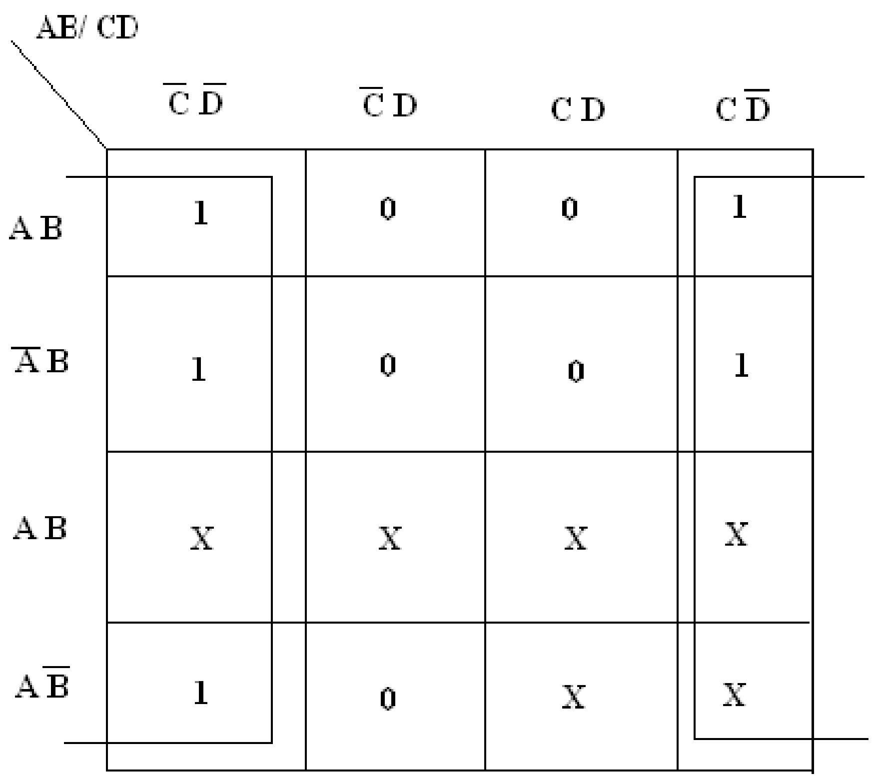
$W = BD + AD + AB' + BC$



$X = BC'D' + B'D + B'C$



$Y = CD + \bar{C}\bar{D}$



$Z = D'$

NAND gate implementation for simplified function

W = BD + AD + AB' + BC

By complementing twice we get

W = ((BD + AD + AB' + BC)')'

= ((BD)' . (AD)' . (AB')' . (BC)')'

X = BC'D + B'D + B'C

By complementing twice we get

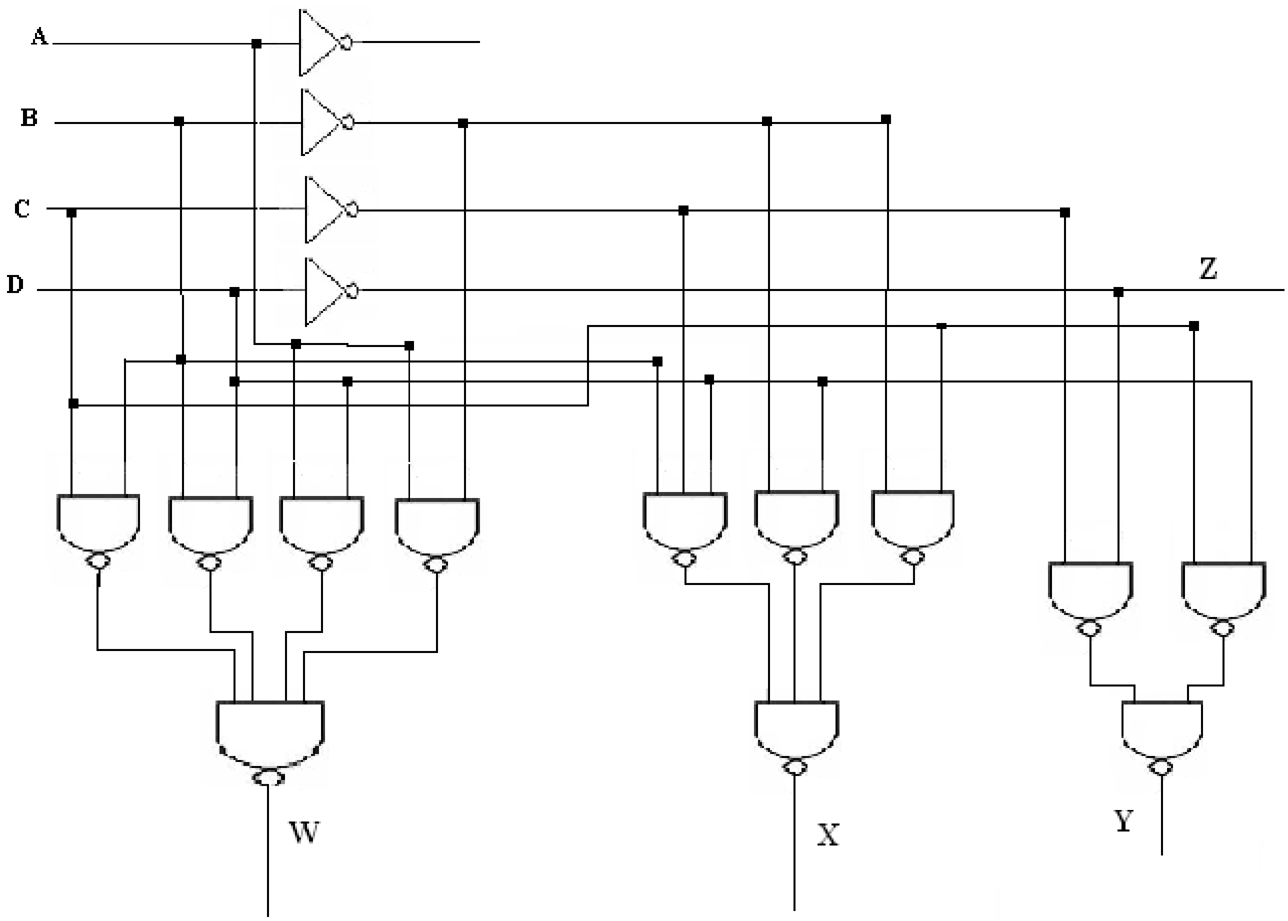
X = BC'D + B'D + B'C

= ((BC'D)' . (B'D)' . (B'C)')'

Y = C'D' + CD

= ((C'D')' + (CD)')'

Z = D'



Logic diagram for BCD to excess 3 code converter by using minimum number of NAND gates

Q.57 With the help of a suitable diagram, explain how do you convert a JK flipflop to T type flipflop. **(4)**

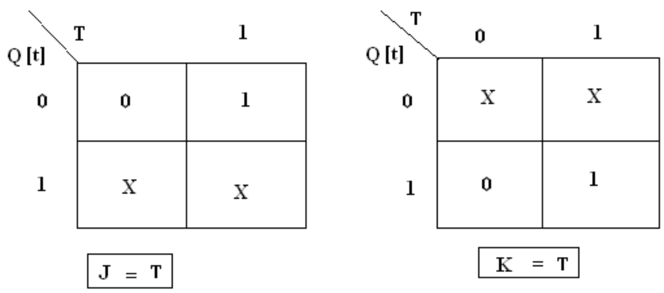
Ans:

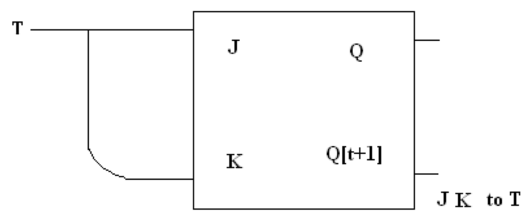
Given flip flop is JK flip flop and it is required to convert JK into T. First we draw the characteristic table of T flip flop and then relate the transition with excitation table of JK flip flop.

Q[t]	T	Q[T+1]	J	K
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	1

Excitation Table JK Flip Flop			
Q[t]	Q[t+1]	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Now we solve K maps for J and K by considering T and Q(t) as input.





Logic diagram convert a JK flipflop to T type flipflop.

Q.58 A number of 256 x 8 bit memory chips are available. To design a memory organization of 2 K x 8 memory. Identify the requirements of 256 x 8 memory chips and explain the details. **(8)**

Ans:

Chips available=256x8

Required capacity=2048x8

Number of chips=(2048x8)/(256x8)=8=(256=2^8)

Address lines required for 2048x8chip=11(2048=2^{11})

Thus the size of the decoder=3x8

Q.59 Convert $(177.25)_{10}$ to octal. **(8)**

Ans:
$(177.25)_{10} = (\quad\quad)_8$
First we take integer part

8	177	**1**
8	22	**6**
8	2	**2**
	0	

(remainders read from bottom to top)

Thus $(177)_{10} = (261)_8$

Now as 0.25 x 8 = 2.00
and 0.00 x 8 = 0
Thus $(0.25)_{10} = (0.2)_8$
Therefore, Thus $(177.25)_{10} = (261.2)_8$

Q.60 Perform the following subtraction using 1's complement
(i) 11001 – 10110 (ii) 11011 - 11001 **(8)**

Ans:
(i) 11001 – 10110 = X – Y

X = 11001
1's complement of Y = 01001
Sum = 1 00010
End around carry = 1
So X-Y = 00011

(ii) 11011 – 11001 = X – Y

X = 11011
1's complement of Y = 00110
Sum = 1 00001
End around carry = 1
So X-Y = 00010

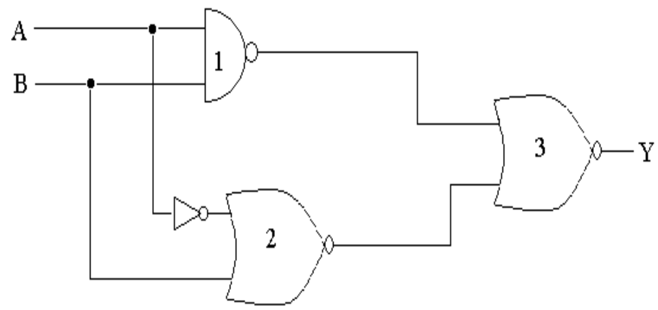
Q.61 Prove the following identities
(i) $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\overline{B}\,\overline{C} + A\,B\,\overline{C} = \overline{C}$
(ii) $A\,B + A\,B\,C + \overline{A}\,B + A\,\overline{B}\,C = B + A\,C$ **(8)**

Ans:
(i) LHS = A'B'C' + A'BC' + AB'C' + ABC'
= A'C' (B' + B) + AC' (B' + B)
= A'C' + AC' [as B'+B = 1]
= C' (A' + A)
= C' [as A'+A =1]

= **RHS.**
Hence Proved

(ii) LHS = AB + ABC + A'B + AB'C = B + AC
= B (A + A') + AC (B + B')
= B + AC [as B + B' = A + A' = 1]
= B + AC
= **RHS.**
Hence Proved

Q.62 Find the boolean expression for the logic circuit shown below. **(8)**



Ans:

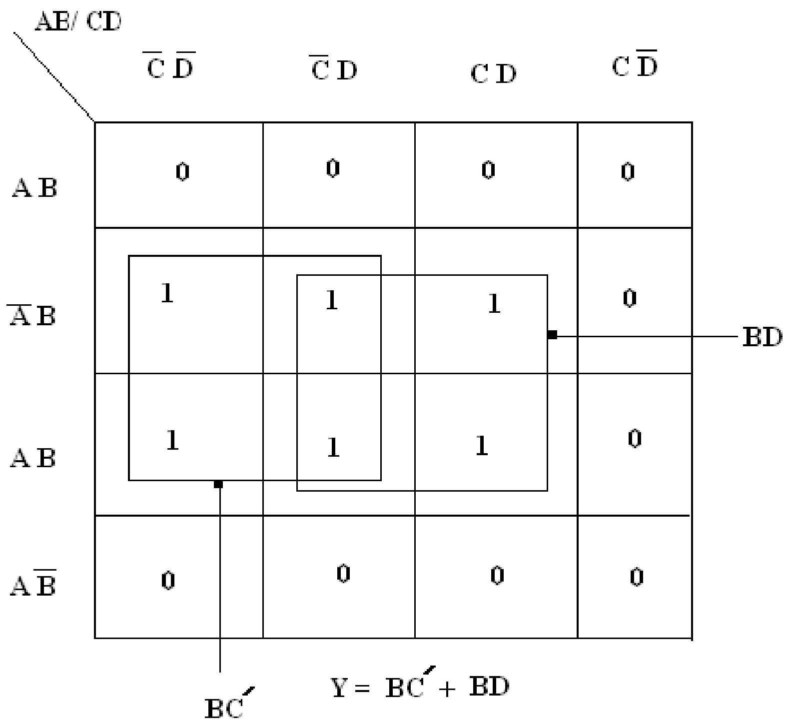
Output of Gate-1 (NAND) = (AB)'
Output of Gate-2 (NOR) = (A'+B)'
Output of Gate-3 (NOR) = [(AB)' + (A'+B)']'
Now applying De-Morgans law, (X+Y)' = X'Y'
and (XY)' = (X'+Y')
[(AB)' + (A'+B)']' = [(AB)']' [(A'+B)']'
= (AB) (A'+B)
= AA'B + ABB
= ABB
= AB.

Q.63 Reduce the following equation using k-map

$Y = B\overline{C}\,\overline{D} + \overline{A}B\overline{C}D + AB\overline{C}D + \overline{A}BCD + ABCD$ **(8)**

Ans:

Multiplying the first term by (A+A')
Y = A'BC'D' + ABC'D' + A'BC'D + ABC'D + A'BCD + ABCD
= $\sum(4,12,5,7,15,13)$
= BC' + BD



Q.64 Implement the following function using 8 to 1 multiplexer

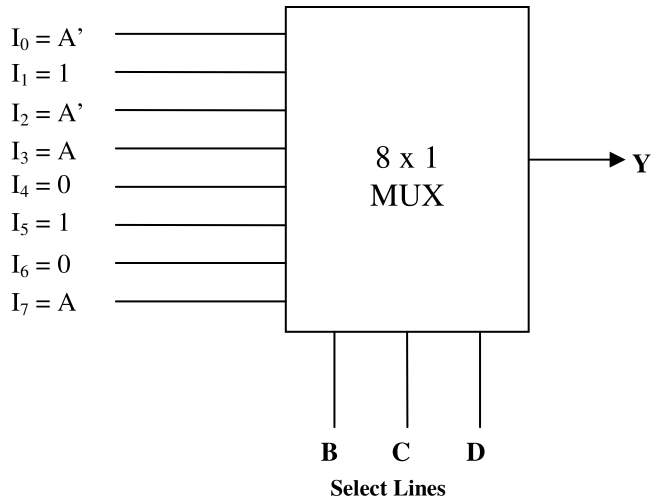
$$Y(A,B,C,D)=\sum(0,1,2,5,9,11,13,15)$$ **(8)**

Ans:

We will take three variables B,C & D at selection lines and A as input. Now there are eight inputs and they can be 0,1,A or A' depending on the Boolean function.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	A'	1	A'	A	0	1	0	A

Now, the realization is:



Q.65 (i) How many 128×8 RAM chips are required to provide a memory capacity of 2048 bytes.

(ii) How many lines of address bus must be used to access 2048 bytes of memory. How many lines of these will be common to each chip?

(iii) How many bits must be decoded for chip select? What is the size of decoder? **(8)**

Ans:

(i) Available RAM chips = 128 x 8

Required memory capacity = 2048 x 8

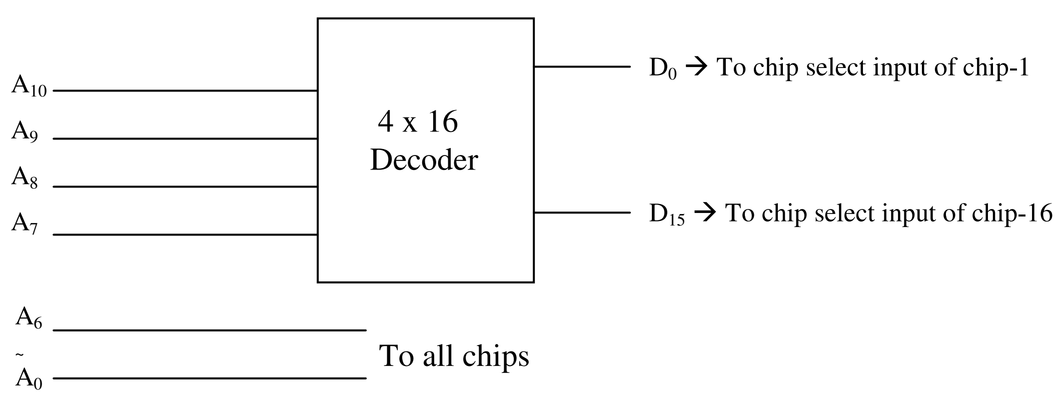
Number of chips required = (2048 x 8) / (128 x 8)

= 16.

(ii) Chips available are of 128 x 8 in size. It means that total 128 (2^7) locations are there and each location can store 8 bits. Thus the total number of address lines required to access 128 locations is 7. As seven address lines can address 2^7 locations. These seven lines are common to all chips.

Now to access 2048 locations, we require 11 address lines, as 2048 = 2^{11}

(iii) These higher order lines will be applied to decoder input. The number of inputs to the decoder will be 11 - 7 = 4. The size of the decoder will be 4x16. These 16 decoder outputs will be connected to the chip select input of individual chips.



Q.66 How many bits are required at the input of a ladder D/A converter, if it is required to give a resolution of 5mV and if the full scale output is +5V. Find the %age resolution. **(8)**

Ans:

First we find out the ratio of Full scale output to Resolution = 5V / 5 mV = 1000.
Now number of bits = $\log_2 1000 = 10$.
Percentage Resolution = 5 mV / 5 V * 100 = 0.1%

Q.67 A 6-bit Dual Slope A/D converter uses a reference of –6V and a 1 MHz clock. It uses a fixed count of 40 (101000). Find Maximum Conversion Time. **(4)**

Ans

The time T_1 given by
$T_1 = 2^N T_C$ where N = no. of Bits, T_c = time period of clock pulse
Given N = 6, T_C = 1/ 1MHz = 1 µs.
Therefore $T_1 = 2^6 \times 10^{-6}$ s = 64 µs.

Q.68 A 2-digit BCD D/A converter is a weighted resistor type with $E_R = 1$ Volt, with $R = 1M\Omega$, $R_f = 10K\Omega$. Find resolution in Percent and Volts. **(5)**

Ans

Resolution = $1/2^2$ = 0.25 volts.
As the resolution is determined by number of input bits of D/A converter; For example two bit converter has 2^2 (4) possible output levels, therefore its resolution is 1 part in 4
In percent it will be ¼ X 100 = 25%
In volts, it will be 0.25 volts.

PART – III

DESCRIPTIVES

Q.1 Distinguish between min terms and max terms. **(6)**

Ans: Distinguish between Minterms and Maxterms:

(i) Each individual term in standard Sum Of Products form is called as minterm whereas each individual term in standard Product Of Sums form is called maxterm.
(ii) The unbarred letter represent 1's and the barred letter represent 0's in min terms, whereas the unbarred letter represent 0's and the barred represent 1's in maxterms.
(iii) If a system has variables A, B, C then the minterms would be in the form ABC, whereas the maxterm would be in the form A+B+C.
(iv) The minterm designation for three variable expression be

$$Y=\sum m\,(1, 3, 5, 7)$$

Where the capital $\sum$ represents the product and m stands for minterms.
Decimal number 1 corresponds to binary number 001 or $\overline{A}\,\overline{B}C$
Decimal number 3 corresponds to binary number 011 or $\overline{A}BC$
Decimal number 5 corresponds to binary number 101 or $A\overline{B}C$
Decimal number 7 corresponds to binary number 111 or ABC.
Whereas the Maxterm designation for three variable expression be

$$Y=\prod M\,(0, 1, 3, 4)$$

Where the capital $\prod$ represents the product and M stands for maxterms.
Decimal 0 means binary 000 and term is A+B+C
Decimal 1 means binary 001 and term is $A+B+\overline{C}$
Decimal 3 means binary 011 and term is $A+\overline{B}+\overline{C}$
Decimal 4 means binary 100 and term is $\overline{A}+B+C$

Q.2 What are universal gates. Construct a logic circuit using NAND gates only for the expression x = A . (B + C). **(7)**

Ans:
Universal Gates: NAND and NOR Gates are known as Universal gates. The AND, OR, NOT gates can be realized using any of these two gates. The entire logic system can be implemented by using any of these two gates. These gates are easier to realize and consume less power than other gates.
Construction of a logic circuit for the expression X = A (B + C) using NAND gates is Shown in fig.4 (b)

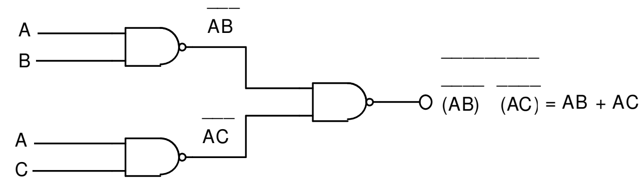


Fig.4(b) Logic Diagram for the expression X = A (B + C)

Q.3 Mention the various IC logic families. **(7)**

Ans:

Various IC Logic Families: Digital IC's are fabricated by employing either the Bipolar or the Unipolar Technologies and are referred to as Bipolar Logic Family or Unipolar Logic Family

I Bipolar Logic Families:

There are two types of operations in Bipolar Logic Families

1. Saturated Logic Families
2. Non-saturated Logic Families

1. Saturated Logic Families: In Saturated Logic, the transistors in the IC are driven to saturation.

(i) Resistor-Transistor Logic (RTL).
(ii) Direct-Coupled Transistor Logic (DCTL)
(iii) Integrated-Injection Logic (I^2L)
(iv) Diode -Transistor Logic (DTL)
(v) High-Threshold Logic (HTL)
(vi)Transistor-Transistor Logic (TTL)

2. Non-saturated Logic: In Non-saturated Logic, the transistors are not driven into saturation.

(i) Schottky TTL
(ii) Emitter Coupled Logic (ECL)

II Unipolar Logic Families:

MOS devices are Unipolar devices and only MOSFETs are employed in MOS logic circuits. The MOS logic families are

(i) PMOS
(ii) NMOS, and
(iii) CMOS

while in PMOS only p-channel MOSFETs are used and in NMOS only n-channel MOSFETs are used, in complementary MOS (CMOS), both P and N channel MOSFETs are employed and are fabricated on the same silicon chip.

Q.4 What is a half-adder? Explain a half-adder with the help of truth-table and logic diagram. **(10)**

Ans:

Half Adder: A logic circuit for the addition of two one-bit numbers is referred to as an half-adder. The addition process is illustrated in truth table shown in Table 6.1. Here A and B are the two inputs and S (SUM) and C (CARRY) are two outputs.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 6.1 Truth Table for Half Adder

From the truth table, we obtain the logical expressions for S and C outputs as

$$S = \overline{A}B + A\overline{B}$$

$$C = AB$$

The logic diagram for an Half-adder using gates is shown in fig.6(a)

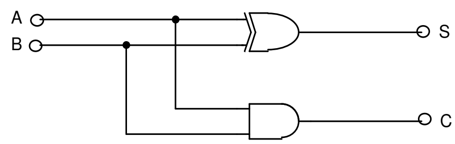


Fig.6(a) Logic Diagram for an Half-adder

Q.5 Using a suitable logic diagram explain the working of a 1-to-16 de multiplexer.**(7)**

Ans:

Working of a 1-to-16 Demultiplexer: A demultiplexer takes in data from one line and directs it to any of its N outputs depending on the status of the selected inputs. If the number of output lines is N (16), the number of select lines m is given by $2^m = N$.i.e., $2^4 = 16$. So, the number of select lines required for a 1-to-16 demultiplexer is 4. Table 7.1 shows the Truth Table of 1-to-16 Demultiplexer. The input can be sent to any of the 16 outputs, D_0 to D_{15}. If DCBA = 0000, the input goes to D_0. If DCBA = 0001, the input goes to D_1 and so on.

Fig.7(a) shows the logic diagram of a 1-to-16 demultiplexer, consists of 8 NOT gates, 16 NAND gates, one data input line(G), 4 select lines (A,B,C,D) and 16 output lines (D_0, D_1, D_2 ------D_{16}). The 8 NOT gates prevent excessive loading of the driving source. One data input line G is implemented with a NOR gate used as negative AND gate. A low level in each input $\overline{G_1}$ and $\overline{G_2}$ is required to make the output G high. The output G of enable is one of the inputs to all the 16 NAND gates. G must be high for the gates to be enabled. If the enable gate is not activated then all sixteen de multiplexer outputs will be high irrespective of the state of the select lines A,B,C,D.

Demulti-plexer Input	Selection Lines D C B A	Logic Function	Demultiplexer Outputs D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
0	0 0 0 0	$\overline{D}\,\overline{C}\,\overline{B}\,\overline{A}$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0 0 0 1	$\overline{D}\,\overline{C}\,\overline{B}\,A$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0 0 1 0	$\overline{D}\,\overline{C}\,B\,\overline{A}$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0 0 1 1	$\overline{D}\,\overline{C}\,B\,A$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	0 1 0 0	$\overline{D}\,C\,\overline{B}\,\overline{A}$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	0 1 0 1	$\overline{D}\,C\,\overline{B}\,A$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	0 1 1 0	$\overline{D}\,C\,B\,\overline{A}$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	0 1 1 1	$\overline{D}\,C\,B\,A$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1 0 0 0	$D\,\overline{C}\,\overline{B}\,\overline{A}$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1 0 0 1	$D\,\overline{C}\,\overline{B}\,A$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1 0 1 0	$D\,\overline{C}\,B\,\overline{A}$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1 0 1 1	$D\,\overline{C}\,B\,A$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
12	1 1 0 0	$D\,C\,\overline{B}\,\overline{A}$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
13	1 1 0 1	$D\,C\,\overline{B}\,A$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
14	1 1 1 0	$D\,C\,B\,\overline{A}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	1 1 1 1	$D\,C\,B\,A$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Table 7.1 Truth Table of 1-to-16 Demultiplexer

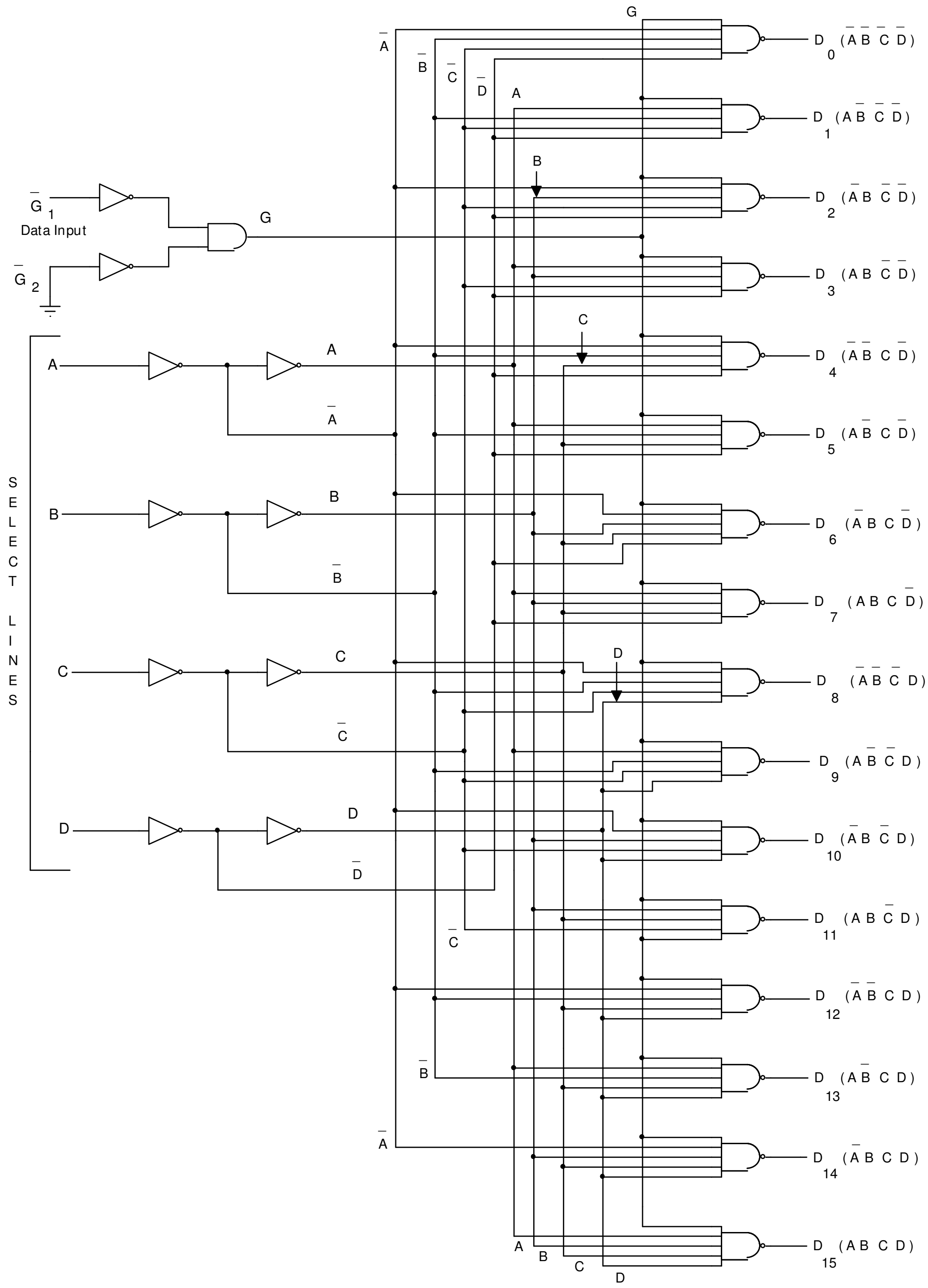


Fig.7(a) Logic Diagram of 1-to-16 De multiplexer

Q.6 . With relevant logic diagram and truth table explain the working of a two input EX-OR gate. **(7)**

Ans:

Two-Input EX-OR Gate: An Exclusive-OR (EX-OR) gate recognizes words which have an odd number of ones. Fig.7(b) shows the logic diagram of an EX-OR gate and Fig.7(c) shows the symbol of an EX-OR Gate. The upper AND gate gives an output $\overline{A}$ B and the lower AND gate gives an output A $\overline{B}$.

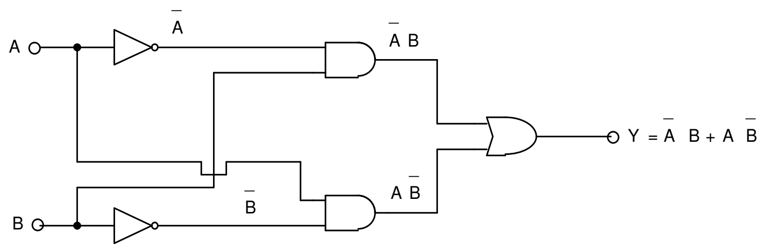


Fig.7(b) Logic Diagram of EX-OR Gate

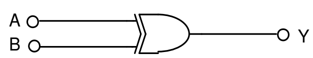


Fig.7(c) Symbol of EX-OR Gate

Therefore, the output equation becomes Y = $\overline{A}$ B + A $\overline{B}$ = A EX-OR B = A ⊕ B
If both A and B are low, the output is low. If either A or B (not both) are high (and the other is low), the output is high. If both A and B are high, output is low. Thus the output is 1 when A and B are different. Table 7.2 shows the Truth Table for EX-OR gate.

A	**B**	**Y ($\overline{A}$ B + A $\overline{B}$)**
0	0	0
0	1	1
1	0	1
1	1	0

Table 7.2 Truth Table of EX-OR Gate

Q.7 With the help of clocked JK flip flops and waveforms, explain the working of a three bit binary ripple counter. Write truth table for clock transitions. **(14)**

Ans:

3-Bit Binary Ripple Counter: In Ripple Counters, all the Flip-Flops are not clocked simultaneously and the flip-flops do not change state exactly at the same time. A 3-bit

Binary Counter has maximum of 2^3 states i.e., 8 states, which requires 3 Flip-Flops. The word Binary Counter means a counter which counts and produces binary outputs 000,001,010--111.It goes through a binary sequence of 8 different states (i.e, from 0 to 7). Fig.8(a) shows the logic circuit of a 3-bit Binary Ripple Counter consisting of 3 Edge Triggered JK flip-flops. As indicated by small circles at the CLK input of flip-flops, the triggering occurs when CLK input gets a negative edge. Q_0 is the Least Significant Bit (LSB) and Q_2 is the Most Significant Bit (MSB). The flip-flops are connected in series. The Q_0 output is connected to CLK terminal of second flip-flop. The Q_1 output is connected to CLK terminal of third flip-flop. It is known as a Ripple Counter because the carry moves through the flip-flops like a ripple on water.

Working: Initially, CLR is made Low and all flip-flops Reset giving an output Q = 000. When CLR becomes High, the counter is ready to start. As LSB receives its clock pulse, its output changes from 0 to 1 and the total output Q = 001. When second clock pulse arrives, Q_0 resets and carries (i.e., Q_0 goes from 1 to 0 and, second flip flop will receive CLK input). Now the output is Q = 010. The third CLK pulse changes Q_0 to 1 giving a total output Q = 011. The fourth CLK pulse causes Q_0 to reset and carry and Q_1 also resets and carries giving a total output Q = 100 and the process goes on. The action is shown is Table 8.1.The number of output states of a counter are known as Modulus (or Mod). A Ripple Counter with 3 flip-flops can count from 0 to 7 and is therefore, known as Mod-8 counter.

Counter State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table.8.1 Counting Sequence of a 3-bit Binary Ripple Counter

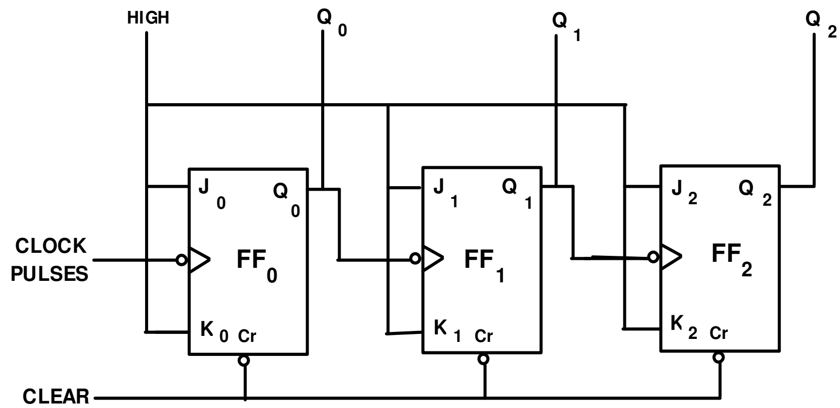


Fig.8(a) Logic Diagram of 3-Bit Binary Ripple Counter

Ripple counters are simple to fabricate but have the problem that the carry has to propagate through a number of flip flops. The delay times of all the flip flops are added. Therefore, they are very slow for some applications. Another problem is that unwanted pulses occur at the output of gates.

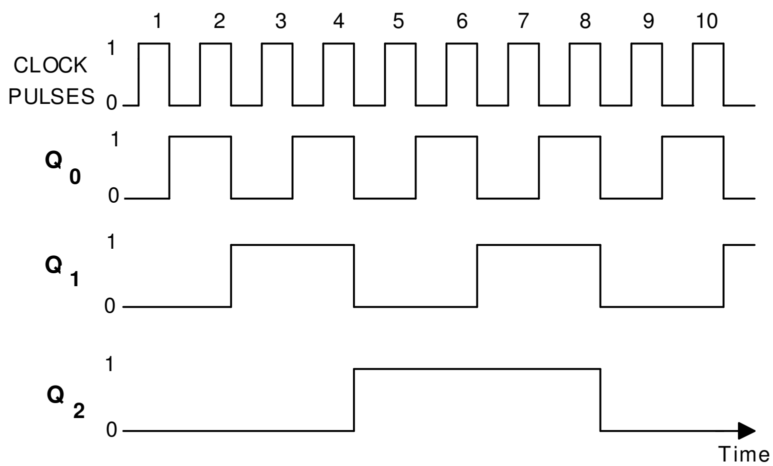


Fig.8(b) Timing Diagram of 3-bit Binary Ripple Counter

The timing diagram is shown in *Fig.8(b)*. FF_0 is LSB flip flop and FF_2 is the MSB flip flop. Since *FF0* receives each clock pulse, Q_0 toggles once per negative clock edge as shown in Fig. 8*(b)*.The remaining flip flops toggle less often because they receive negative clock edge from preceding flip flops. When Q_0 goes from 1 to 0, FF_1 receives a negative edge and toggles. Similarly, when Q_1 changes from 1 to 0, FF_2 receives a negative edge and toggles. Finally when Q_2 changes from 1 to 0, FF_3 receives a negative edge and toggles. Thus whenever a flip flop resets to 0, the next higher flip flop toggles.
This counter is known as ripple counter because the 8th clock pulse is applied, the trailing edge of 8th pulse causes a transition in each flip flop. Q_0 goes from High to Low, this causes Q_1 go from High to Low which causes Q_2 to go from High to Low which causes Q_3

to go from High to Low. Thus the effect ripples through the counter. It is the delay caused by this ripple which result in a limitation on the maximum frequency of the input signal.

Q.8 Using D-Flip flops and waveforms explain the working of a 4-bit SISO shift register. **(14)**

Ans:

Serial In - Serial Out Shift Register: Fig.9(a) shows a 4 bit serial in - serial out shift register consisting of four D flip flops FF_0 , FF_1 , FF_2 and FF_3. As shown it is a positive edge triggered device. The working of this register for the data 1010 is given in the following steps.

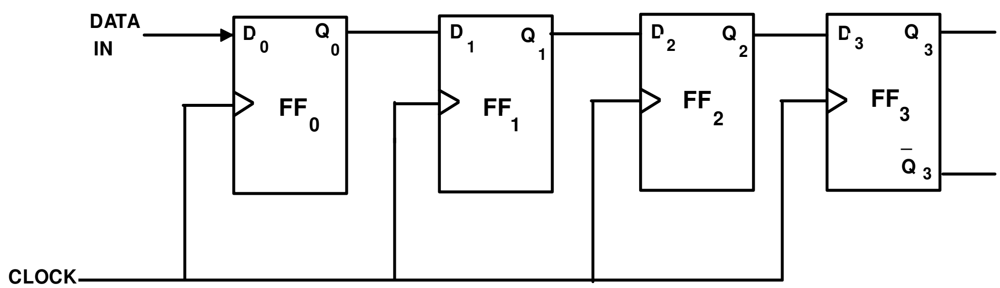


Fig.9(a) Logic Diagram of 4-bit Serial In – Serial Out Shift Register

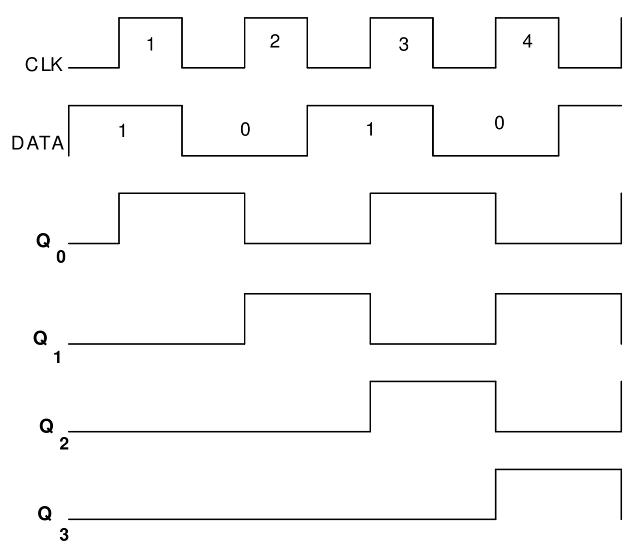


Fig.9(b) Output Waveforms of 4-bit Serial-in Serial-out Register

1. Bit 0 is entered into data input line. $D_0 = 0$, first clock pulse is applied, FF_0 is reset and stores 0.
2. Next bit 1 is entered. $Q_0 = 0$, since Q_0 is connected to D_1, D_1 becomes 0.
3. Second clock pulse is applied, the 1 on the input line is shifted into FF_0 because FF_0 sets. The 0 which was stored in FF_0 is shifted into FF_1.
4. Next bit 0 is entered and third clock pulse applied. 0 is entered into FF_0, 1 stored in FF_0 is shifted to FF_1 and 0 stored in $FF1$ is shifted to FF_2.
5. Last bit 1 is entered and 4th clock pulse applied. 1 is entered into FF_0, 0 stored in FF_0 is shifted to FF_1, 1 stored in FF_1 is shifted to FF_2 and 0 stored in $FF2$ is shifted to FF_3.

This completes the serial entry of 4 bit data into the register. Now the LSB 0 is on the output Q_3.

6. Clock pulse 5 is applied. LSB 0 is shifted out. The next bit 1 appears on Q_3 output.
7. Clock pulse 6 is applied. The 1 on Q_3 is shifted out and 0 appears on Q_3 output.
8. Clock pulse 7 is applied. 0 on Q_3 is shifted out. Now 1 appears on Q_3 output.
9. Clock pulse 8 is applied. 1 on Q_3 is shifted out.
10. When the bits are being shifted out (on CLK pulse 5 to 8) more data bits can be entered in.

Q.9 With the help of R-2R binary ladder, explain the working of a 4-bit D/A converter **(14)**

Ans:

R-2R Ladder network method: In a R-2R ladder network method of digital to analog conversion, irrespective of number of bits of the DAC only two convenient values of resistors are needed in the ratio of 1:2 as depicted in fig 10(a). An R-2R Ladder Network based on constant reference current. In the circuit of fig 10(a) points G are actual ground and points G' are virtual ground. Therefore the potential at all the G_s and G'_s is zero. Between ground (actual or virtual) and node A there are two resistors each of value 2R in parallel. Therefore this resultant resistance between ground and node A is R and the current through each of the 2R resistance connected to node A must be same. Let us say this current is I. Then the current flowing from A to B through the resistor R is 2I. Then the total resistance from ground to node B through the node A becomes 2R. Also the resistance directly connected between ground and B is also 2R. So between the node B and ground there are two equal resistances in parallel each of value 2R. Therefore, the resultant resistance is R and the current approaching to node B from both sides must be equal. Since current approaching from the side of node A is 2I, therefore the current approaching to the node B from the resistor 2R under it must also be 2I. Hence the total current approaching the node C from the side of node B is 4I. On the basis of the same logic the current approaching to node D from the side of node C must be 8I and the current approaching it form the 2R resistor under node D should also be 8I.

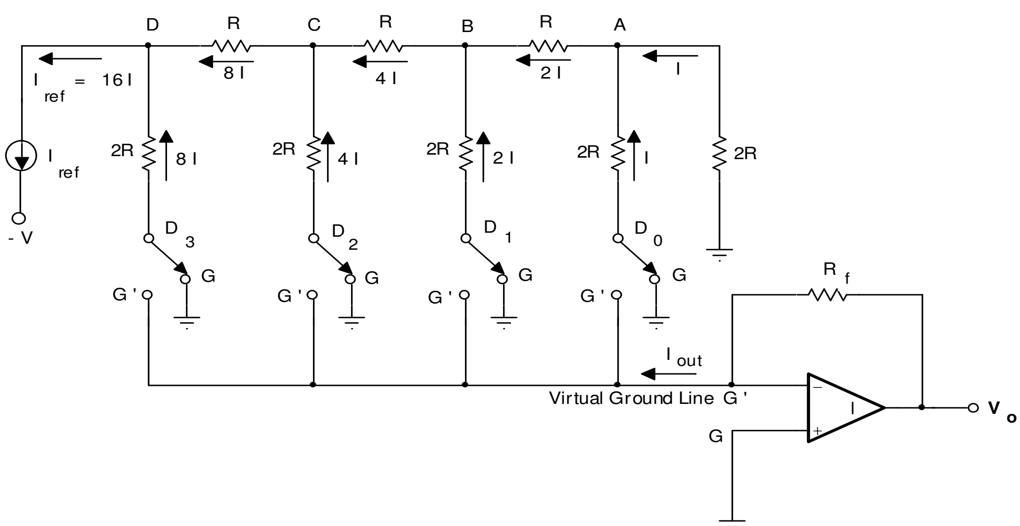


Fig.10(a) R-2R Ladder Network D/A Converter

Whenever any of the bit or bits of the digital input word D_3 D_2 D_1D_0 is high, the corresponding transistor switch is ON *i.e.* connected to virtual ground and the current of that vertical branch of the ladder comes from the output, otherwise the current of the vertical branch comes directly from the actual ground without any effect on the output. Hence the output current (lout) gives the analog current value corresponding to the digital input word. This analog current gets converted to the analog voltage V_o.

An R-2R 4-Bit Ladder Network DAC based on reference voltage: An R-2R 4-bit Ladder Network D/A Converter is shown in fig. 10(b)

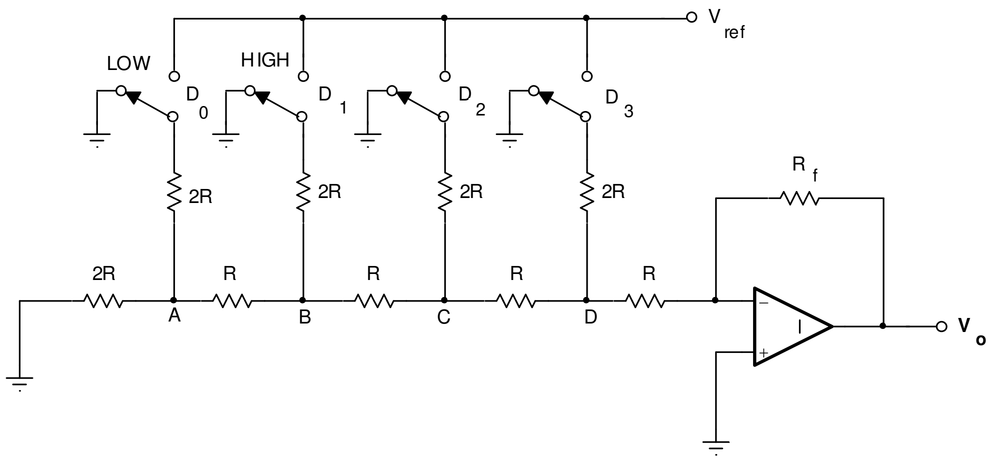


Fig.10(b) R-2R 4-bit Ladder Network D/A Converter

Proof:

Step 1: If the digital value to be converted to analog value is 0001 *i.e.*D_0 is on the high side connected to V_{ref} while D_1, D_2, and D_3 are connected to ground. Then the circuit redrawn as shown inFig.10(c).

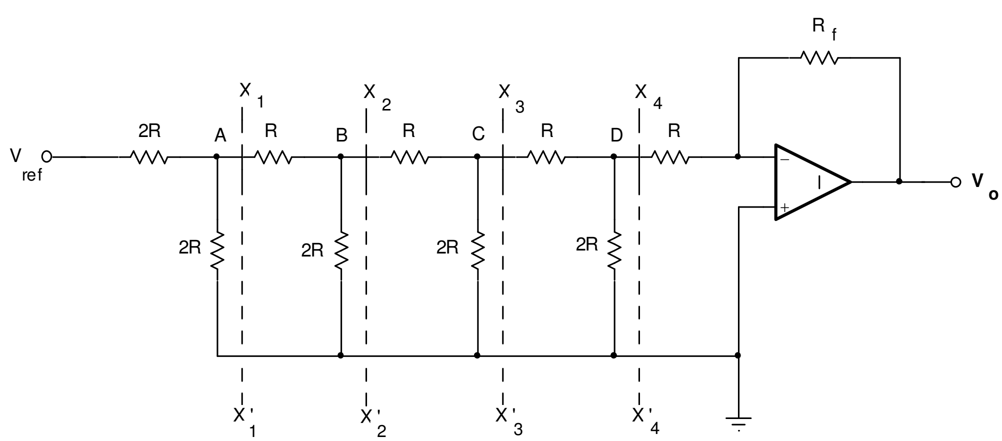


Fig.10(c) R-2R Ladder Network D/A Converter when D_0 is connected to V_{ref} and D_1,D_2,D_3 are connected to ground

Applying Thevenin's theorem at X_1,X_1' , the circuit of fig.10(c) becomes the equivalent circuit shown in fig.10(d)

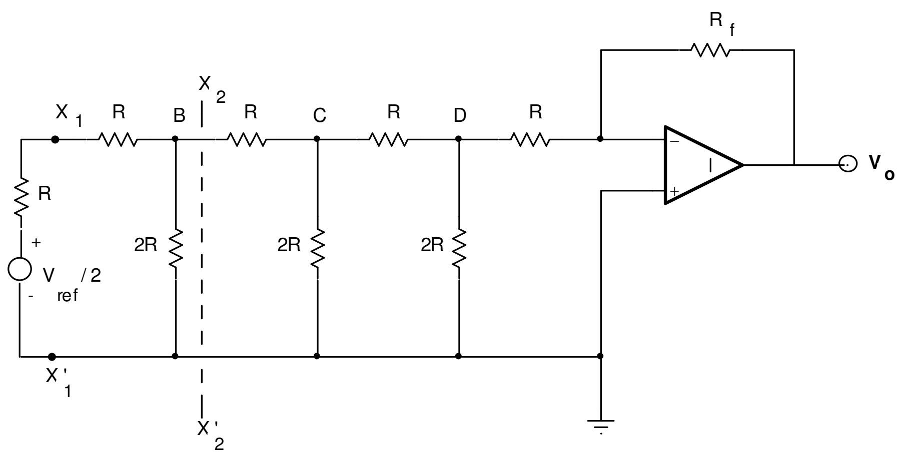


Fig.10(d) R-2R Ladder Network D/A Converter when Thevenin's Theorem applied at X_1 and X_1'

Again Applying Thevenin's Theorem at X_2,X_2', then the circuit of fig.10(d) becomes the equivalent circuit shown in fig.10(e).

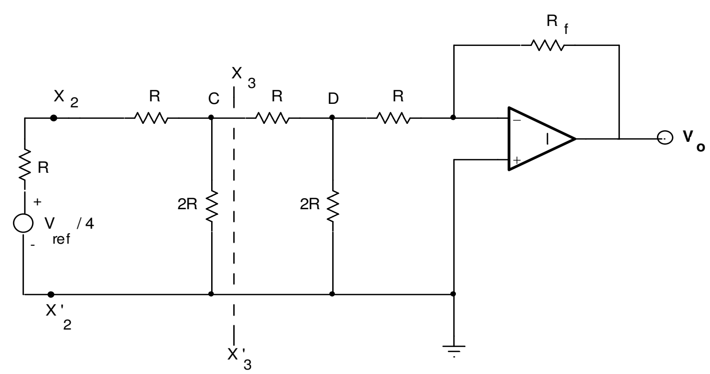


Fig.10(e) R-2R Ladder Network D/A Converter when Thevenin's Theorem applied at X_2 and X_2'

Again Applying Thevenin's Theorem at X_3,X_3' the circuit of fig.10(e) becomes the equivalent circuit shown in fig.10(f):

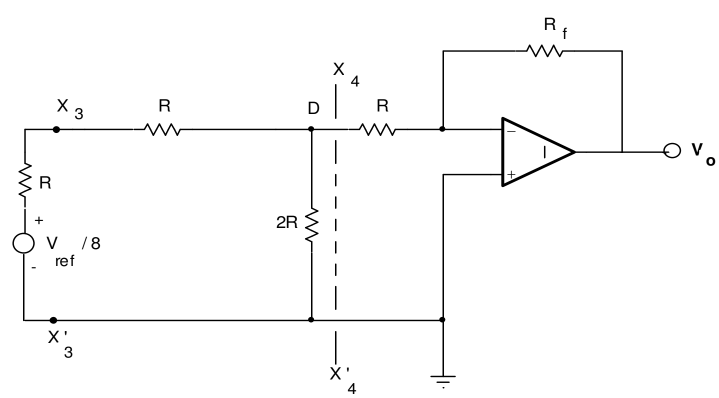


Fig.10(f) R-2R Ladder Network D/A Converter when Thevenin's Theorem applied at X_3 and X_3'

Once Again applying Thevenin's theorem at section X_4, X_4' the circuit of fig.10(f) finally becomes the equivalent circuit shown in fig.10(g).

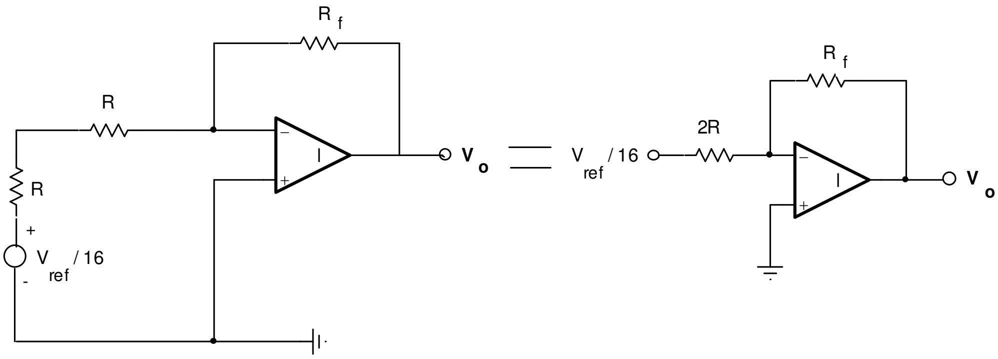


Fig.10(g) R-2R Ladder Network D/A Converter when Thevenin's Theorem applied at X_4 and X_4'

Step 2: If D_1 is high (connected to V_{ref}) and D_0, D_2, D_3 are all low (connected to ground), then the circuit becomes:

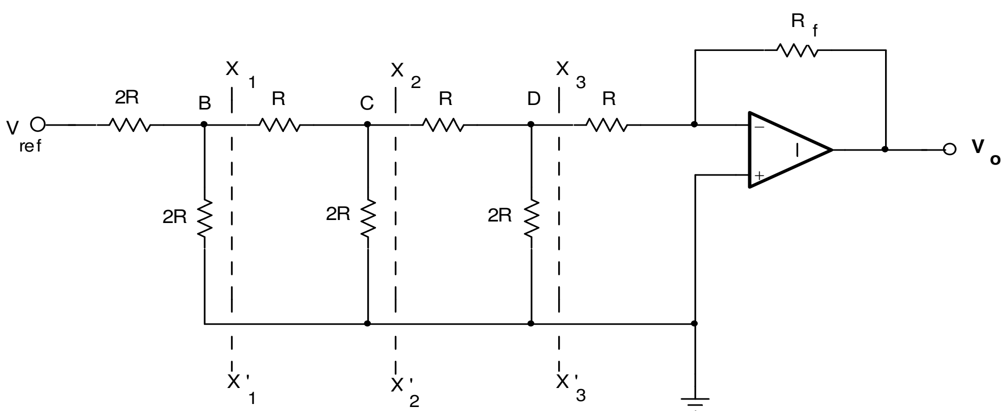


Fig.10(h) R-2R Ladder Network D/A Converter when D_1 is connected to V_{ref} and D_0,D_2,D_3 are connected to ground

Applying Thevenin's Theorem, three times and reducing the circuit each time at sections X_1, X_2, X_3 we finally get the circuit as shown in fig.10(i).

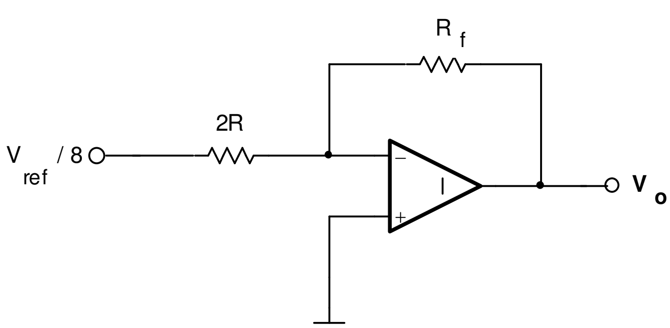


Fig.10(i) Equivalent Circuit when D_1 is connected to V_{ref} D_0,D_2,D_3 are connected to ground

Step 3: Repeating the same exercise of D_2 High and other bits Low, we get the finally reduced Circuit as shown in fig.10(j).

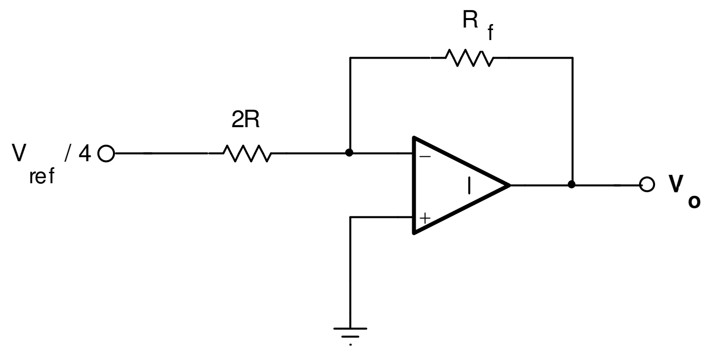


Fig.10(j) Equivalent Circuit when D_2 is connected to V_{ref} D_0,D_1,D_3 are connected to ground

Step 4: Repeating the same for D_3 High and other bits Low, we can reduce the circuit shown in fig.10(k).

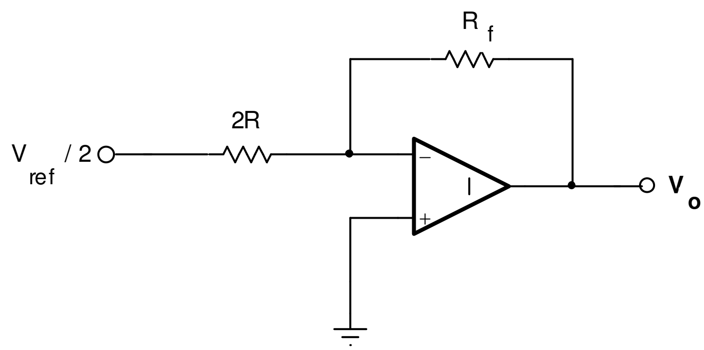


Fig.10(k) Equivalent Circuit when D_3 is connected to V_{ref} D_0,D_1,D_2 are connected to ground

Step 5: Compiling the reduced circuits of the above four steps by applying Superposition Theorem, then the network of fig 10(g),10(i),10(j),10(k) becomes the equivalent circuit shown in fig.10(m).

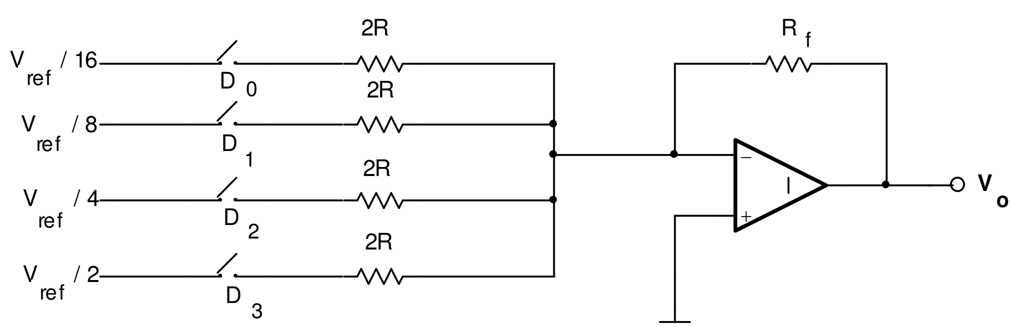


Fig.10(m) Equivalent circuit by applying Superposition Theorem for the circuits of fig.10(g),10(i),10(j),10(k)

Hence the derived equivalent circuit of the R-2R ladder network proves that the bits of the input digital word D_3, D_2, D_1, D_0 receive the applied voltages as per their binary weights and we get the corresponding analog value at V_o. Therefore,

$$V_O = \frac{V_{ref}}{2R}.R_f\left(\frac{D_3}{2}+\frac{D_2}{4}+\frac{D_1}{8}+\frac{D_0}{16}\right)$$

$$V_O = \frac{V_{ref}}{2R}.R_f\left(\frac{D_{n-1}}{2}+\frac{D_{n-2}}{4}+.....+\frac{D_0}{2^n}\right)$$

If R_f is also selected equal to 2R, then

$$V_O = V_{ref}.\left(\frac{D_{n-1}}{2}+\frac{D_{n-2}}{4}+.....+\frac{D_0}{2^n}\right)$$

V_O is independent of the numerical values of R. Thus any convenient value of R & 2R can be taken for the design of the D/A converter. The maximum output analog voltage is nearly equal to V_{ref}. The actual values of R-2R resistors influence only the maximum current handled by the op-amp. Voltage resolution of n-bit ladder network DAC is $V_{ref}/2^n$

Q.10 With relevant diagram explain the working of master-slave JK flip flop. **(9)**

Ans:

Master-Slave *J-K* FLIP-FLOP: A master-slave *J-K* FLIP-FLOP is a cascade of two *S-R* FLIP-FLOPS. One of them is known as Master and the other one is slave. Fig.11(a) shows the logic circuit. The master is positively clocked. Due to the presence of inverter, the slave is negatively clocked. This means that when clock is high, the master is active and the slave is inactive.

When the clock is low, the master is inactive and the slave is active. Fig.11(b) shows the symbol. This is a level clocked Flip-Flop. When clock is high, any changes in J and K inputs can affect S and R outputs. Therefore, J and K are kept constant during positive half of clock. When clock is low, the master is inactive and J and K inputs can be allowed to be changed. The different conditions are Set, Reset, and Toggle. The race condition is avoided because of feedback from slave to master and the slave being inactive during positive half of clock.

(i) **SET State**: Assume that Q is low (and $\overline{Q}$ is high). For high J, low K and high CLK, the Master goes to SET state giving High S and Low R. Since Slave is inactive, Q and $\overline{Q}$ do not change. When CLK becomes Low, the Slave becomes to Set state giving High Q (and low $\overline{Q}$).

(ii) **RESET State**: At the end of Set State Q is High (and $\overline{Q}$ low). Now if J is low, K is high and CLK is high, the Master Resets giving Low S and High R. Q and $\overline{Q}$ do not change because Slave is inactive. When CLK becomes Low, the Slave becomes active and resets giving Low Q (and High $\overline{Q}$).

(iii) Toggle State: If both J and K are High, the Slave copies the Master. When CLK is High, the Master toggles once. Then the Slave toggles once when CLK is low. If the Master toggles into Set state, the slave copies the Master and toggles into Set state. If the Master toggles into Reset state, the slave again copies the Master and toggles into Reset state. Since the second FLIP-FLOP simply follows the first one, it is referred to as the *slave* and the first one as the *master*. Hence, this configuration is referred to as *master-slave(M-S) FLIP*-FLOP.

Truth Table of JK Master Slave Flip-Flop in Table 11.1 shows that a Low PR and Low CLR can cause race condition. Therefore, PR and CLR are kept High when inactive. To clear, we make CLR Low and to preset we make PR Low. In both cases we change them to High when the system is to be run.

Low J and Low K produce inactive state irrespective of clock input. If K goes High, the next clock pulse resets the Flip-Flop. If J goes High by itself, the next clock pulse sets the Flip-Flop. When both J and K are High, each clock pulse produces one toggle.

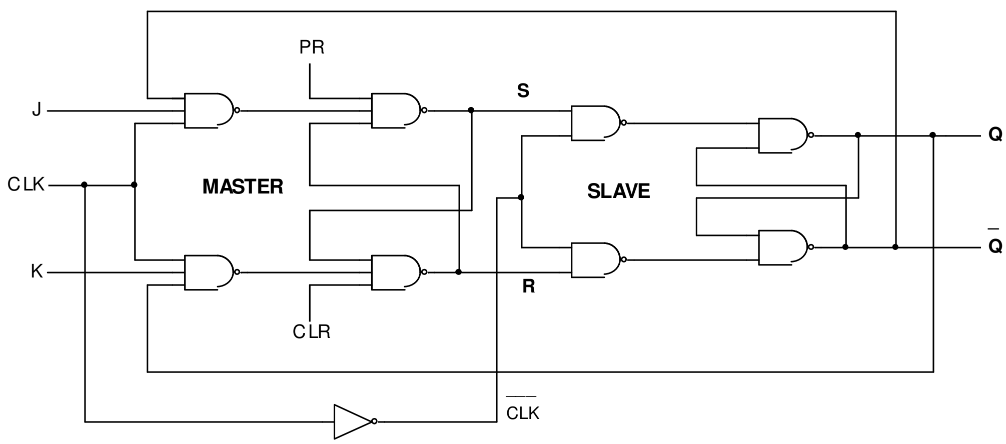


Fig.11(a) Logic Diagram of Master-Slave J-K FLIP-FLOP

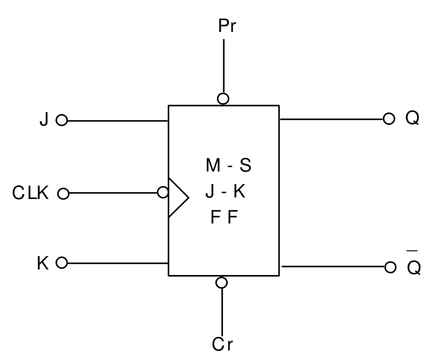


Fig.11(b) Logic Symbol of Master-Slave J-K FLIP-FLOP

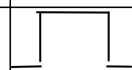
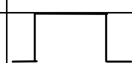
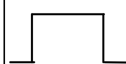
		Inputs			Output
PR	CLR	CLK	J	K	Q
0	0	X	X	X	Race Condition
0	1	X	X	X	1
1	0	X	X	X	0
1	1	X	0	0	No change
1	1		0	1	0
1	1		1	0	1
1	1		1	1	Toggle

Table 11.1 Truth Table of JK Master-Slave Flip-Flop

Q.11 Compare the memory devices RAM and ROM. **(5)**

Ans:

Comparison of Semi-conductor Memories ROM and RAM

The advantages of ROM are:

1. It is cheaper than RAM.
2. It is non-volatile. Therefore, the contents are not lost when power is switched off.
3. It is available in larger sizes than RAM. '
4. It's contents are always known and can be easily tested.
5. It does not require refreshing.
6. There is no chance of any accidental change in its contents.

The advantages of RAM are:

1. It can be updated and replaced.
2. It can serve as temporary data storage.
3. It does not require lead time (as in ROM) or programming time (as in PROM).
4. It does not require any programming equipment

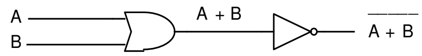
Q.12 State and prove Demorgan's laws. **(5)**

Ans:

De Morgan's Theorems:

(i) Statement of First Theorem: $\overline{A+B} = \overline{A} \cdot \overline{B}$

Proof: The two sides of the equation $\overline{A+B} = \overline{A}\,\overline{B}$ is represented by logic diagrams shown in fig.3 (a) & 3(b)



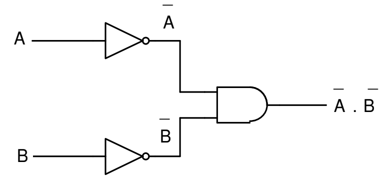


Fig.3(a) Logic diagram for $\overline{A+B}$ **Fig.3(b) Logic diagram for $\overline{A}\,\overline{B}$**

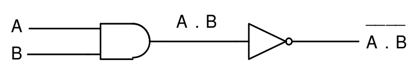
The equality of the logic diagrams of fig.3 (a) & 3(b) is proved by the truth table shown in table 2(c)

Inputs		**Intermediate Values**			**Outputs**	
A	B	A + B	$\overline{A}$	$\overline{B}$	$\overline{A+B}$	$\overline{A}\ \overline{B}$
0	0	0	1	1	1	1
0	1	1	1	0	0	0
1	0	1	0	1	0	0
1	1	1	0	0	0	0

Table 2(c)

(ii) Statement of second theorem: $\overline{AB} = \overline{A} + \overline{B}$

Proof: The two sides of the equation $\overline{AB} = \overline{A} + \overline{B}$ is represented by the logic diagrams shown in fig.3(c) & 3(d).



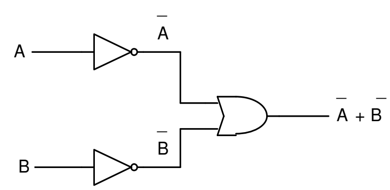


Fig.3(c) Logic diagram for $\overline{AB}$ **Fig.3(d) Logic diagram for $\overline{A} + \overline{B}$**

The equality of the logic diagrams of fig.3(c) & 3(d) is proved by the truth table shown in table 2(d)

Inputs		**Intermediate Values**			**Outputs**	
A	B	A .B	$\overline{A}$	$\overline{B}$	$\overline{A.B}$	$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
0	1	0	1	0	1	1
1	0	0	0	1	1	1
1	1	1	0	0	0	0

Table 2(d)

Q.13 Discuss in detail, the working of Full Adder logic circuit and extend your discussion to explain a binary adder, which can be used to add two binary numbers. **(14)**

Ans:

Full-Adder: A half-adder has only two inputs and there is no provision to add a carry from the lower order bits when multibit addition is performed. For this purpose, a third input terminal is added and this circuit is used to add A_n, B_n, and C_{n-1}, where A_n and B_n are the nth order bits of the numbers, A and B respectively and C_{n-1} is the carry generated from the addition of (n-1)th order bits. This circuit is referred to as full-adder and its truth table is given in Table 5.1

Inputs			Outputs	
A_n	B_n	C_{n-1}	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 5.1 Truth Table of a Full-Adder

The K-maps for the outputs S_n and C_n are given in Fig.5(a) and Fig.5(b) respectively and the minimized expressions are given by

$S_n = \overline{A_n} B_n \overline{C_{n-1}} + \overline{A_n} \, \overline{B_n} C_{n-1} + A_n \overline{B_n} \, \overline{C_{n-1}} + A_n B_n C_{n-1}$

$C_n = A_n B_n + B_n C_{n-1} + A_n C_{n-1}$

	$\overline{A_n}\,\overline{B_n}$	$\overline{A_n} B_n$	$A_n B_n$	$A_n \overline{B_n}$
$\overline{C_{n-1}}$		1		1
C_{n-1}	1		1	

Fig.5(a) K-map for S_n

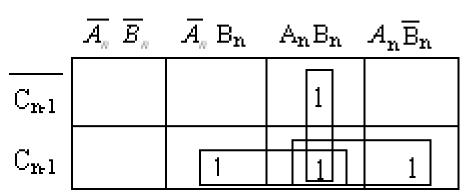


Fig.5(b) K-map for C_n

The logic diagrams for the Sn and Cn are shown in fig.5(c) & fig.5(d).

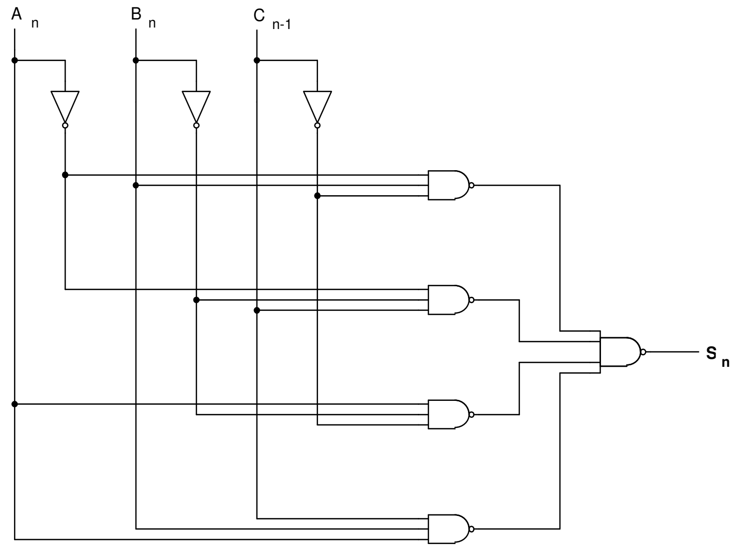


Fig.5(c) NAND-NAND Realization of S_n

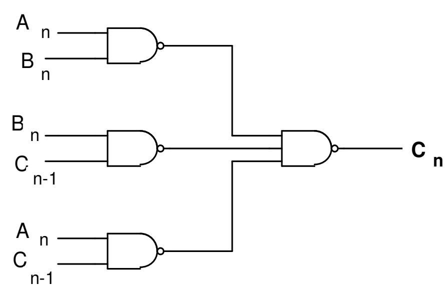


Fig.5(d) NAND-NAND Realization of C_n

Binary Adder: The full adder forms the sum of two bits and a previous carry. Two binary numbers of n bits each can be added by means of Binary Adder. If A = 1011 and B = 0011, whose sum is S = 1110. When pair of bits is added through a full-adder, the circuit produces a carry to be used with the pair of bits one significant position higher. This is shown in Table 5.2 The bits are added with full-adders, starting from the Least Significant Position (subscript 1), to form the sum bit and carry bit. The input carry C1 in the Least Significant position must be 0. The value of C_{i+1} in a given significant position is the output carry of the full-adder. This value is transferred into the input carry of the full-adder that adds the bits one higher significant position to the left. The sum bits are thus generated starting form the rightmost position and are available as soon as the corresponding previous carry bit is generated

Subscript i	4	3	2	1		Full-Adder
Input Carry	0	1	1	0	C_i	Z
Augend	1	0	1	1	A_i	X
Addend	0	0	1	1	B_i	Y
Sum	1	1	1	0	S_i	S
Output Carry	0	0	1	1	C_{i+1}	C

Table 5.2 Truth Table for Binary Adder

A Binary Parallel Adder is a digital function that produces the arithmetic sum of two binary numbers in parallel. It consists of full-adders connected in cascade, with the output carry from one full-adder connected to the input carry of the next full-adder. Fig.5(e) shows a 4-bit Binary Parallel Adder. The augend bits of A and the addend bits of the B are designated by subscript numbers from right to left, with subscript 1 denoting the low-order bit. The carries are connected in a chain through the full-adders. The input carry to the adder is C_1 and the output carry is C_5. The S outputs generate the required sum bits.

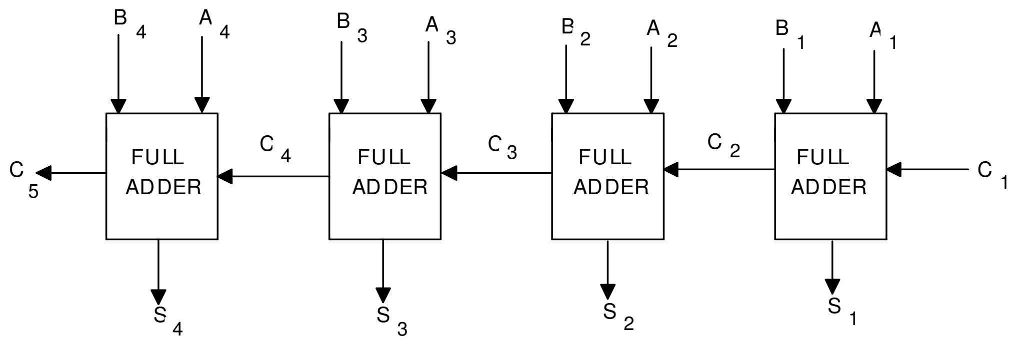


Fig.5(e) 4-bit Binary Parallel Adder using Full-Adders

Q.14 What is a decoder? Draw the logic circuit of a 3 line to 8 line decoder and explain its working. **(7)**

Ans:

Decoder: A Decoder is a combinational logic circuit that converts Binary words into alphanumeric characters. Thus the inputs to a decoder are the bits 1, 0 and their combinations. The output is the corresponding decimal number. It converts binary information from *n* input lines to a maximum of 2^n unique output lines. If the *n-bit* decoded information has unused or don't-care combinations, the decoder output will have less than 2^n outputs.

Working: The logic circuit of a 3 line to 8 line decoder is shown in fig.6 (a). The three inputs (x, y, z) are decoded into eight outputs (from D_0 to D_7), each output representing one of the minterms of the 3-input variables. The three inverters provide the complement of the inputs, and each one of the eight AND gates generate one of the minterms. A particular application of this decoder is a binary-to-octal conversion. The input variables may represent a binary number, and the outputs will then represent the eight digits in the octal number system. However, a 3-to-8 line decoder can be used for decoding any 3-bit code to provide eight outputs, one for each element of the code.

The operation of the decoder may be verified from its input-output relationships shown in Table 6.1.The table shows that the output variables are mutually exclusive because only one output can be equal to 1 at any one time. Consider the case when X=0, Y=0 and Z=0, the output line D_0 (X’, Y’, Z’) is equal to 1 represents the minterm equivalent of the binary number presently available in the input lines.

Inputs			Outputs							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	**1**	0	0	0	0	0	0	0
0	0	1	0	**1**	0	0	0	0	0	0
0	1	0	0	0	**1**	0	0	0	0	0
0	1	1	0	0	0	**1**	0	0	0	0
1	0	0	0	0	0	0	**1**	0	0	0
1	0	1	0	0	0	0	0	**1**	0	0
1	1	0	0	0	0	0	0	0	**1**	0
1	1	1	0	0	0	0	0	0	0	**1**

Table 6.1 Truth Table of 3-to-8 line Decoder

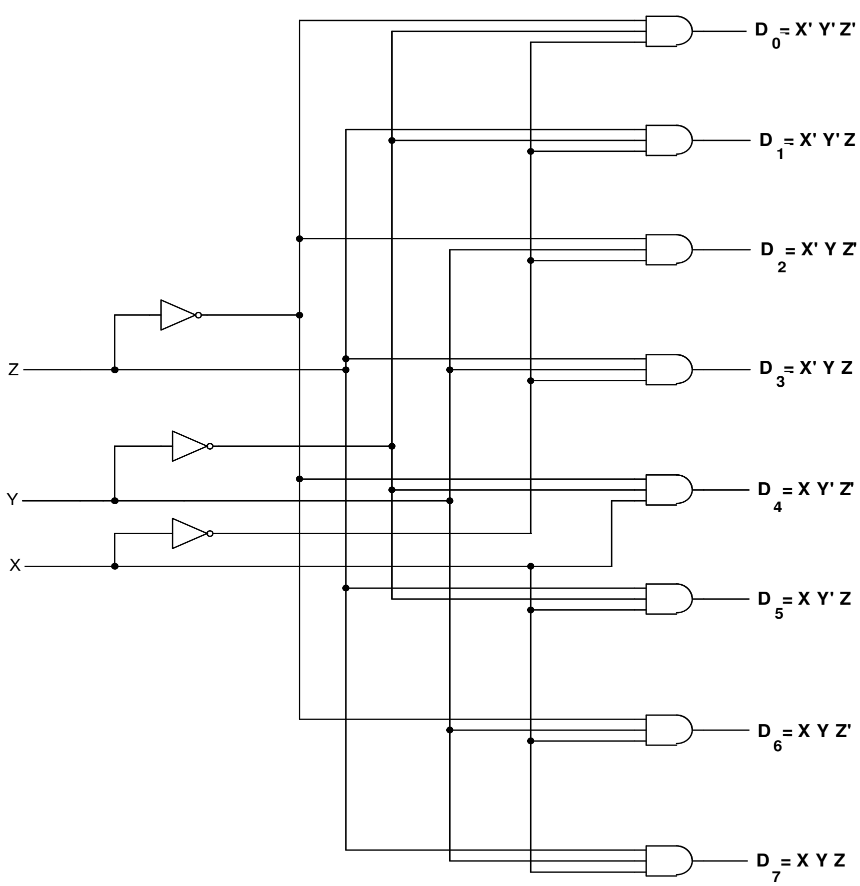


Fig. 6(a) Logic Circuit of 3-to-8 line Decoder

Q.15 What is an encoder? Draw the logic circuit of Decimal to BCD encoder and explain its working. **(7)**

Ans:

Encoder: An Encoder is a combinational logic circuit which converts Alphanumeric characters into Binary codes. It has 2n (or less) input lines and n output lines. An Encoder may be Decimal to Binary, Hexadecimal to Binary, Octal to BCD etc.

Decimal to BCD Encoder: This encoder has 10 inputs (for decimal numbers 0 to p) and 4 outputs for the BCD number. Thus it is a 10 line to 4 line encoder. Table 6(a) lists the decimal digits and the equivalent BCD numbers. From the table, we can find the relationship between decimal digit and BCD bit. MSB of BCD bit is Y_3. For decimal digits 8 or 9, $Y_3 = 1$. Thus we can write OR expression for Y_3 bit as

$$Y_3 = 8 + 9$$

Similarly , Bit Y_2 is 1 for decimal digits 4,5,6 and 7. Thus we can write OR expression

$$Y_2 = 4 + 5 + 6 + 7$$
$$Y_1 = 2 + 3 + 6 + 7$$
$$Y_o = 1 + 3 + 5 + 7 + 9$$

The logic circuit for the expressions (Y0, Y1, Y2, Y3) is shown in fig. 6(b). When a High appears on any of input lines the corresponding OR gates give the BCD output. For *e.g.,* if decimal input is 8, High appears only on output 3 (and LOW on Y_0, Y_1 , Y_2), thus giving the BCD code for decimal 8 as 1000. Similarly, if decimal input is 7, then High appears on outputs Y_0, Y_1, Y_2 (and LOW on $Y3$), thus giving BCD output as 0111.

Decimal Digit	**BCD Code**			
	Y_3	**Y_2**	**Y_1**	**Y_0**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

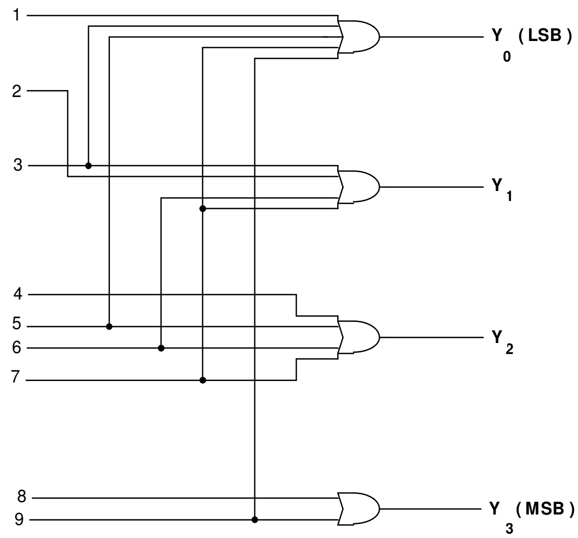


Fig.6(b) Logic diagram for Decimal to BCD Encoder

Q.16 What is a flip-flop? What is the difference between a latch and a flip-flop? List out the application of flip-flop. **(4)**

Ans:

Flip-Flop: A flip-flop is a basic memory element used to store one bit of information. Both Flip-flops and latches are bistable logic circuits and can reside in any of the two stable states due to a feedback arrangement. The main difference between them is in the method used for changing the state.

Applications of Flop-Flops:

(1) Bounce elimination switch
(2) Parallel Data Storage in Registers
(3) Transfer of Data from one bit to another.
(4) Counters
(5) Frequency Division

Q.17 Draw the circuit diagram of a Master-slave J-K flip-flop using NAND gates. What is race around condition? How is it eliminated in a Master-slave J-K flip-flop. **(10)**

Ans:

Logic Diagram of Master-Slave J-K Flip-Flop using NAND Gates: Fig.7(a) shows the logic diagram of Master-Slave J-K Flip-Flop using NAND gates.

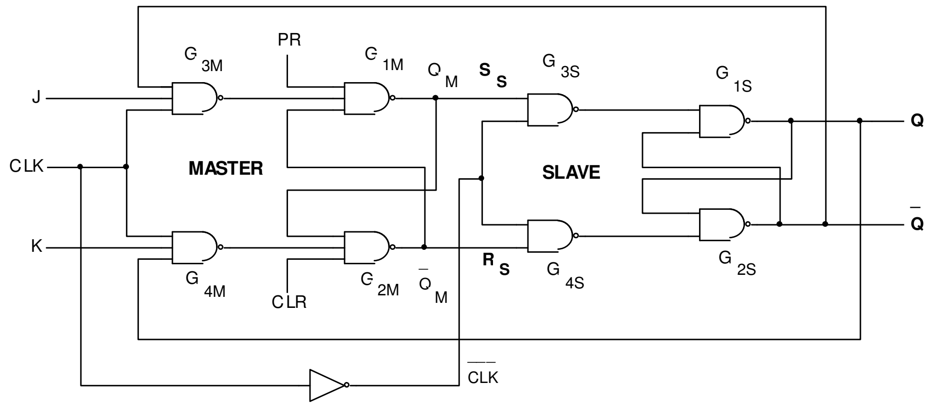


Fig.7(a) Logic Diagram of Master-Slave J-K FLIP-FLOP

<u>The Race-around Condition</u>: The difficulty of both inputs 1 (S = *R* = I) being not allowed in an *S-R* Flip-Flop is eliminated in a *J-K Flip-Flop* by using the feedback connection from outputs to the inputs of the gates. In R-S Flip-Flop, the inputs do not change during the clock pulse *(CK* = 1), which is not true in J-K Flip-Flop because of the feedback connections. Consider that the inputs are $J = K = 1$ and $Q = 0$ and a pulse as shown in Fig. 7(b) is applied at the clock input. After a time interval Δt equal to the propagation delay through two NAND gates in series, the output will change to $Q = 1$.

Now we have $J = K = 1$ and $Q = 1$ and after another time interval of Δt the output will change back to Q = O. Hence, for the duration t_p of the clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock pulse, the value of Q is uncertain. This situation is referred to as the race-around condition.The race-around condition can be avoided if $t_p < \Delta t < T$. However, it may be difficult to satisfy this inequality because of very small propagation delays in ICs. A more practical method of overcoming this difficulty is the use of the master-slave *(M-S)* configuration.

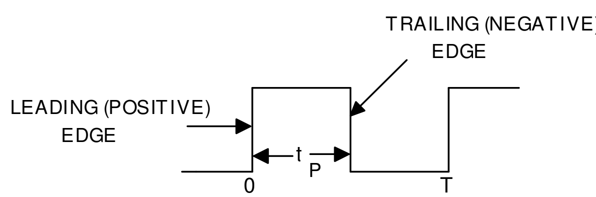


Fig.7 (b) a Clock Pulse

A master-slave J-K Flip-Flop is a cascade of two S-R Flip-Flops with feedback from the outputs of the second to the inputs to the first as illustrated in Fig.7(a). Positive clock pulses are applied to the first Flip-Flop and the clock pulses are inverted before these are applied to the second Flip-Flop. When CK=1, the first Flip-Flop is enabled and the outputs Q_M and $\overline{Q_M}$ respond to their inputs J and K according the Table 7.1. At this time, the second Flip-Flop is inhibited because its clock is LOW ($\overline{CK} = 0$). When CK goes LOW ($\overline{CK} = 1$), the first Flip-Flop is inhibited and the second Flip-Flop is enabled, because now its clock is HIGH ($\overline{CK} = 1$). Therefore, the outputs Q and $\overline{Q}$ Follow the outputs Q_M and $\overline{Q_M}$ respective (second and third rows of Table 7.1). Since the second Flip-Flop simply follows the first one, it is referred to as the Slave and the first one as the Master. Hence, this

configuration is referred to as Master-Slave Flip-Flop. In this circuit, the inputs to the gates G_{3M} and G_{4M} do not change during the clock pulse, therefore the Race-around condition does not exist. The state of the Master-Slave Flip-Flop changes at the negative transition (trailing end).

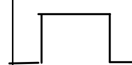
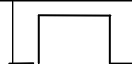
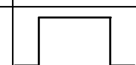
		Inputs			**Output**
PR	CLR	CLK	J	K	Q
0	0	X	X	X	Race Condition
0	1	X	X	X	1
1	0	X	X	X	0
1	1	X	0	0	No change
1	1		0	1	0
1	1		1	0	1
1	1		1	1	Toggle

Table 7.1 Truth Table of JK Master-Slave Flip-Flop

Q.18 What is a demultiplexer? Discuss the differences between a demultiplexer and a decoder. **(4)**

Ans:

Demultiplexer: It is a logic circuit that accepts one data input and distributes it over several outputs. A demultiplexer has one data input, m select lines, and n output lines, whereas a decoder does not have the data input but the select lines are used as input lines.

Q.19 What is a shift register? Can a shift register be used as a counter? If yes, explain how? **(4)**

Ans:

Shift Register: A register in which data gets shifted towards left or right when clock pulses are applied is known as a Shift Register. A shift register can be used as a counter. If the output of a shift register is fed back to serial input, then the shift register can be used as a Ring Counter.

Q.20 What are synchronous counters? Design a Mod-5 synchronous counter using J-K Flip-Flops. **(10)**

Ans:

Synchronous Counters: The term synchronous means that all flip-flops are clocked simultaneously. The clock pulses drive the clock input of all the flip-flops together so that there is no propagation delay.

Mod-5 Counter Synchronous Counter: The Mod-5 Synchronous Counter have five counter states. The counter design table for this counter lists the three flip-flop and their states (0 to 5 states), as shown in table 9(a), the six inputs required for the three flip-flops. The flip-flop inputs required to step up the counter from the present to the next state have been worked out with the help of the excitation table shown in the table.

Input pulse Count	**Counter States**			**Flip-Flop Inputs**					
	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	X	0	X	0	X
1	1	0	0	X	1	1	X	0	X
2	0	1	0	1	X	X	0	0	X
3	1	1	0	X	1	X	1	1	X
4	0	0	1	0	X	0	X	X	1
5(0)	0	0	0						

Table 9(a) counter Design Table for Mod-5 Counter

A flip-flop*:* The initial state is 0. It changes to 1 after the clock pulse. Therefore J_A should be 1 and K_A may be 0 or 1 (that is X).

B flip-flop: The initial state is 0 and it remains unchanged after the clock pulse. Therefore J_B should be 0 and K_B may be 0 or 1 (that is X)

C flip-flop: The state remains unchanged. Therefore Jc should be 0 and K_C should be X.The flip-flop input values are entered in Karnaugh maps shown in Table 9(b) [(i) (ii) (iii) (iv) (v) and (vi)] and a boolean expression is found for the inputs to the three flip-flops and then each expression is simplified. *As* all the counter states have not been utilized, X's (don't) are entered to denote un-utilized states. The simplified expressions for each input shown under each map. Finally, these minimal expressions for the flip-flop inputs are used to draw a logic diagram for the counter, which is shown in fig.9 (b).

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	0	X	1
A	X	X	X	X

(i) Map for J_A

$J_A = \bar{C}$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	X	X	X
A	1	X	X	1

(ii) Map for K_A

$K_A = 1$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	X	X
A	1	X	X	X

(iii) Map for J_B

$J_B = A$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	X	X	0
A	X	X	X	1

(iv) Map for K_B

$K_B = A$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	X	X	0
A	0	X	X	1

(v) Map for J_C

$J_C = AB$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	1	X	X
A	X	1	X	X

(vi) Map for K_C

$K_C = 1$

Table 9(b) Karnaugh Maps for MOD-5 Synchronous Counter

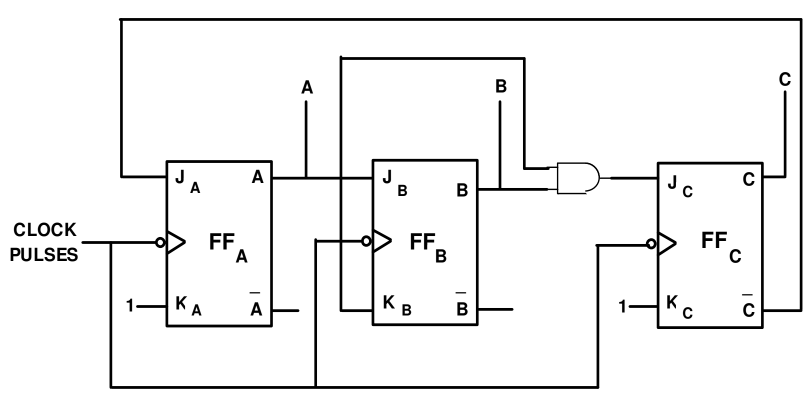


Fig.9 (b) Logic Diagram of MOD-5 Synchronous Counter

Q.21 With the help of a neat diagram, explain the working of a successive approximation A/D converter. **(14)**

Ans:

Successive Approximation ADC:

This is the most widely used A/D converter. As the name suggests, the digital output tends towards analog input through successive approximations. In Successive Approximation ADC, the comparison with the input analog voltage is done in descending order starting from maximum voltage. Fig.10 (a) shows the block diagram of SA A/D converter. The main components are Op-amp Comparator, Control Logic, SA register and D/A converter. It uses Digital to Analog converter as a feedback element. The control logic is the most important part of Successive Approximation Converter, as this decides the next step to be taken. The ring counter provides timing waveform to control the operation of the converter. The Digital to Analog Converter unit, n bit register and ring counter are all reset by the first pulse from the ring counter. The ring counter containing a single one sets the MSB of the Digital to Analog Converter to 1 and the other to 0

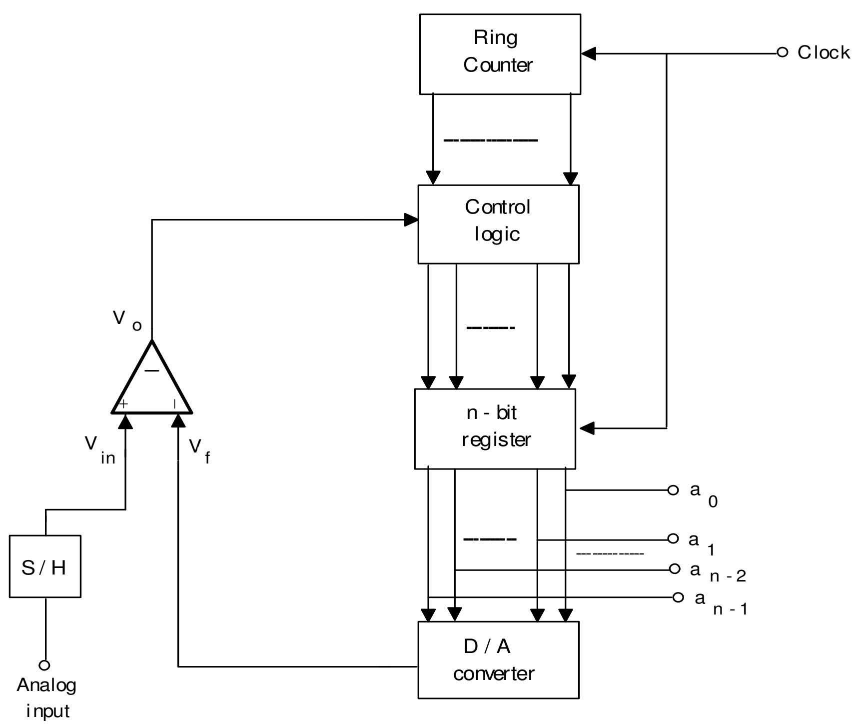


Fig.10 (a) Block Diagram of Successive Approximation A/D Converter

The basic operating principle of Successive Approximation Converter is that the voltage ouput of DAC corresponding to MSB is compared by the comparator with the input voltage and if the voltage is less, the bit 1 is retained. If the voltage is more, it is reset to 0 and counter moves to next position. Similar decisions are made at each bit position until the nearest value is reached.

Assume that the MSB of a unipolar 6 bit converter produces 10 V output and we have to measure an analog output voltage of 8.2 V. Each bit divides the voltage by 2 so that the voltages for the 6 bits from MSB downwards is

Bits	5	4	3	2	1	0
Voltage	10	5	2.5	1.25	0.625	0.3125
	MSB					LSB

The operation of SA A/D converter is shown in Table No.10(a). Let the analog input be 8.2 V. The SA register is first set to zero. Then 10 is placed in MSB. This is fed to D/A converter whose output goes to comparator. Since the analog input (8.2 V) is greater than D/A output (i.e.,10 V), the MSB is set to one. Then 1 is placed in bit next to MSB (i.e., 1 is placed in second position). Now the output of D/A is 5 V. Since analog input is less than 5 V, it is reset to 0. Next 0 is placed in third position. Now the D/A output is (5+2.5=7.5V) which is less than analog input. Therefore, this 0 bit is retained and 0 is placed in the next bit (i.e., fourth position). Now the D/A output is (7.5+1.25=8.75), which is more than analog input. Therefore, the 1 bit is placed in fifth position. Now the D/A output is (8.75+0.625=8.125) which is less than analog input, it is reset to 0. Now 0 is placed in LSB producing a D/A output of (8.125+0.3125=8.4375) which is more than analog input. Therefore, LSB is set to one.

The various steps and voltages are tabulated in Table No.10 (a).

Step	Register	DAC Output	Comparator decision w.r.t 8.2V.
Start	100000	10	High
2	010000	5	Low
3	011000	5+2.5=7.5	Low
4	011100	7.5+1.25=8.75	High
5	011010	7.5+0.625=8.125	Low
6	011011	8.125+0.3125=8.4375	High

Table 10(a)

The D/A converter waveform is shown in fig.10 (b)

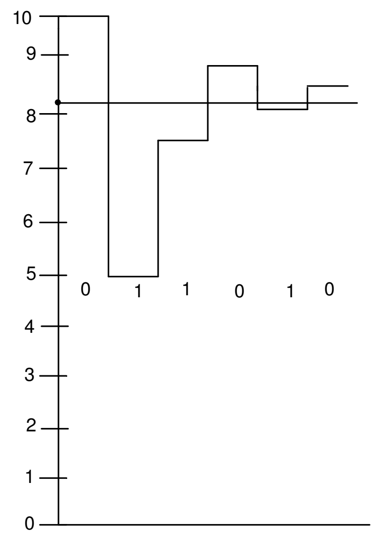


Fig.10 (b) Output Waveform of D/A Converter

Features:

(i) It is one of the most widely used ADC

(ii) Its conversion time is very next only to Flash or Parallel ADC

(iii) SACs have fixed value of conversion time that is not dependent on the value of analog input voltage.

(iv) Data can be taken out either in serial or in parallel.

(v) During the period of comparison the input analog voltage should be held constant and so the input to comparator is through a Sample Hold circuit.

Q.22 Difference between static and dynamic RAM. Draw the circuits of one cell of each and explain its working. **(10)**

Ans:

Differentiation between Static RAM and Dynamic RAM:

Static RAMs store ones and zeros using conventional FLIP-FLOPs. whereas, the memory cells of dynamic RAMs are basically charge storage capacitors with driver transistors.The presence or absence of charge in a capacitor is interpreted as Logic1 or 0.

Static RAMs do not require refreshing because there is no problem of charge leaking-off in FLIP-FLOPs whereas Dynamic RAMs require periodic charge refreshing to maintain data storage because the charge stored on capacitors leak-off with time.

Static RAMs are slower but easier to drive than dynamic memories, which generally require clock signals in addition to extra power supplies whereas dynamic circuits usually require externally generated clock voltages,

Advantages of Static RAMs over Dynamic RAMs:

(i)Higher speed of operation (faster)i.e, lower access –time.

(ii)Does not require refreshing.

Advantages of Static RAMs over Dynamic RAMs:

(i)Higher number of bits storage on a given silicon chip area. i.e, Higher packaging density.

(ii)Lower power consumption.

Static RAM Cell: A RAM memory cell consisting of two cross-coupled MOS inverters is shown in Fig.11 (a). It is addressed by setting A_X and A_Y to 1. When A_X = 1, the cell is connects to the data and $\overline{data}$ line. When A_Y = 1, T_7 and T_8 are ON.
To write into the cell, set W = 1, T_9 becomes ON. If data input is 1, the voltage at node D will correspond to level 1 making T_3 ON and level at $\overline{D}$ will be 0. On the other hand, if the data input is at logic 0, then T_3 will be OFF and $\overline{D}$ would be at 1. To read the state of the FLIP-FLOP, we set R = 1.This connects the data output to $\overline{D}$. Thus, the complement of the data level written into the cell is read at $\overline{data}$ output.

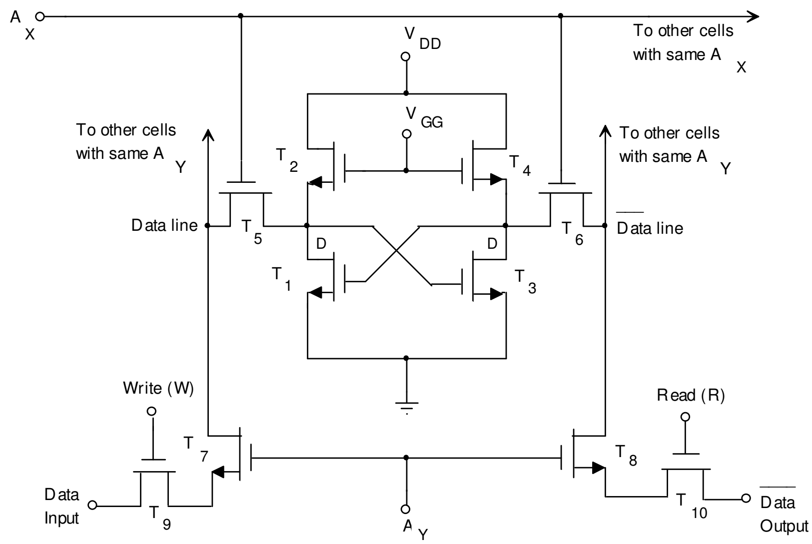


Fig.11(a) Logic Diagram of a Static MOS RAM Cell

Dynamic RAM Cell: A dynamic cell uses four transistors in place of the six used in a static cell. This reduces the silicon chip area and results in saving of power. The circuit of a 4-transistor dynamic MOS RAM cell is shown in Fig.11 (b).The state of the cell is stored on the stray capacitances C_1 and C_2, whose presence is essential. The cell is addressed by making $A_X = A_Y =1$. In one state of the cell, the voltage across C_1 is large and T_1 is ON. Correspondingly, C_2 has zero voltage and T_2 is OFF. In the other state, the voltages on C_1 and C_2 and the conducting states of T_1 and T_2 are reversed. For writing into the cell, we set W = 1 and for reading from the cell we set R = 1.It is necessary to refresh the cell periodically, otherwise the charge stored on the capacitors leak off. The refreshing operation is accomplished by allowing brief access from the supply voltage V_{DD} to the cell. This is done by making A_X = 1 and the refresh terminal voltage corresponding to 1 level. This makes T_3, T_4, T_9, and T_{10} ON. Suppose initially T_1 is ON, T_2 is OFF. The voltage across C_1 is large and across C_2 it is zero volt. During the refresh interval, V_{DD} is applied through T_{10} and T_4 to C_1, since T_2 is OFF. Therefore, current from V_{DD} will flow through C_1, allowing C_1 to replenish any charge lost due to leakage. Since T1 is ON, hence C_2 will not charge as rapidly as C_1. Similarly V_{DD} is applied to C_2, which is in parallel to T_1 when T_1 is OFF and T_2 is ON.

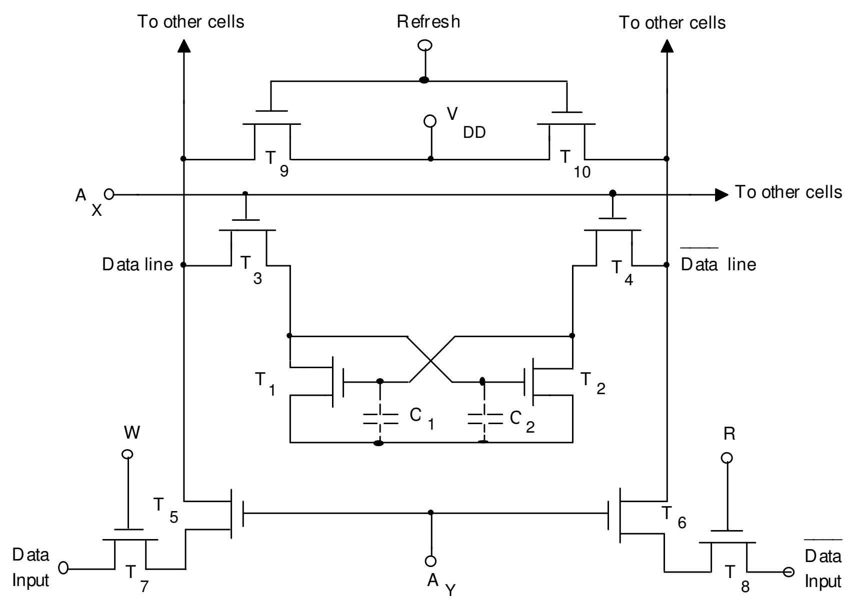


Fig.11(b) Logic Diagram of Dynamic MOS RAM Cell

Q.23 Distinguish between ROM, PROM, EPROM, EEPROM. **(4)**

Ans:

ROM: Read Only Memory is a Permanent Memory. In Permanent ROM, the data is permanently stored and cannot be changed. It can only be read from the memory. There cannot be a write operation because the specified data is programmed into the device by the manufacturer or the user. ROM is a Non-volatile memory. Some examples of ROM are conversion tables, pre-programmed instructions etc.

PROM: Programmable Read Only Memory allows user to store the data. An instrument PROM programmer is used to store the required data. The process used is opening the links at bit locations using high current (this process is called burning in). Once this process has been done, the data is permanently stored and no change is possible.

EPROM: EPROM means Erasable PROM. It can be reprogrammed by first erasing the existing program. EPROM uses N-MOSFET array with isolated gate structure. The isolated transistor gate has no electrical connection and can store an electrical charge indefinitely. The data bits in this memory array are represented by presence or absence of charge. Erasure is achieved by removing the gate charge. EPROM can be UV EPROM or EEPROM.

UV EPROM means Ultra Violet Erasable PROM. Erasure is achieved by using ultra violet light. The light passes through a window in the IC package to the chip where there are stored charges. Thus the stored contents are erased.

EEPROM: EEPROM means Electrically Erasable PROM. In this memory device, the erasure and programming is done by electrical pulses.

Q.24 What is a universal gate? Give examples. Realize the basic gates with any one universal gate. **(8)**

Ans:

Universal Gates: NAND and NOR are known as Universal gates The AND, OR, NOT gates can be realized using any of these two gates. The entire logic system can be implemented by using any of these two gates. These gates are easier to realize and consume less power than other gates.

Realizations of NOT, AND and OR gates using NAND gates

NOT GATE: Fig. 3(a) shows the realization of Inverter (NOT) gate using NAND gate. Both the inputs to the NAND gates are tied together so that the gate works as an inverter (NOT) gate.

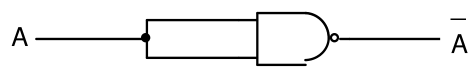


Fig. 3(a) Realization of Inverter (NOT) gate using NAND gate

AND GATE: Fig. 3(b) shows the realization of AND gate using two NAND gates. It has combination of two NAND gates gives AND operation. The first NAND gate has two inputs A and B. The two inputs to the second NAND gate are tied together and the output $\overline{AB}$ of the first gate is fed to this common terminal. The output is AB thus giving AND operation.

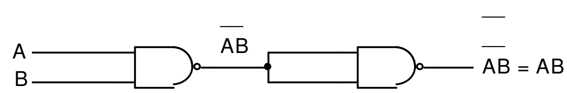


Fig. 3(b) Realization of AND gate using NAND gates

OR GATE: Fig. 3(c) shows the realization of OR gate using NAND gates. The two inputs from each of the first two NAND gates are tied together and fed by A and B as shown in the figure. The outputs are $\overline{A}$ and $\overline{B}$. They are fed to as inputs to third NAND gate. The final output is A OR B thus giving OR operation.

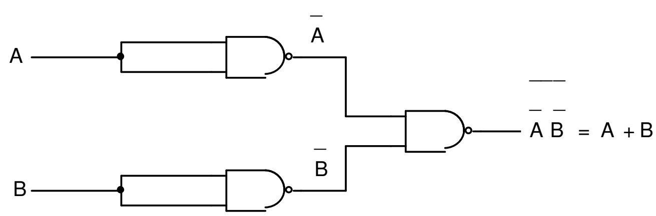


Fig. 3(c) Realization of OR gate using NAND gates

Q.25 Give the circuit of a TTL NAND gate and explain its operation in brief. **(6)**

Ans:

Operation of TTL NAND Gate: Fig.3(d) shows a TTL NAND gate with a totem pole output. The totem pole output means that transistor T_4 sits atop T_3 so as to give low output impedance. The low output impedance implies a short time constant RC so that the

output can change quickly from one state to another. T_1 is a multiple emitter transistor. This transistor can be thought of as a combination of many transistors with a common base and collector. Multiple emitter transistors with about 60 emitters have been developed. In the figure, T_1 has 3 emitters so that there can be three inputs A, B, C. The transistor T_2 acts as a phase splitter because the emitter voltage is out of phase with the collector voltage. The transistors T_3 and T_4 from the totem pole output, The capacitance CL represents the stray capacitance etc. The diode D is added to ensure that T_4 is cut off when output is low. The voltage drop of diode D keeps the base-emitter junction of T_4 reverse biased so that only T_3 conducts when output is low. The operation can be explained briefly by three conditions as given below:

Condition 1: At least one input is low (i.e., 0). Transistor T_1 saturates. Therefore, the base voltage of T_2 is almost zero. T_2 is cut off and forces T_3 to cut off. T_4 acts like an emitter follower and couples a high voltage to load. Output is high (i.e. Y=1).

Condition 2: All inputs are high. The emitter base junctions of T_1 are reverse biased. The collector base junction of T_1 is forward biased. Thus, T_1 is in reverse active mode. The collector current of T1 flows in reverse direction. Since this current is flowing into the base of T_2, the transistors T_2 and T_3 saturate and output Y is low.

Condition 3: The circuit is operating under II when one of the input becomes low. The corresponding emitter base junction of T_1 starts conducting and its base voltage drops to a low value. Therefore, T_1 is in forward active mode. The high collector current of T_1 removes the stored charge in T_2 and T_3 and therefore, T_2 and T_3 go to cutoff and T_1 saturates and output Y returns to high.

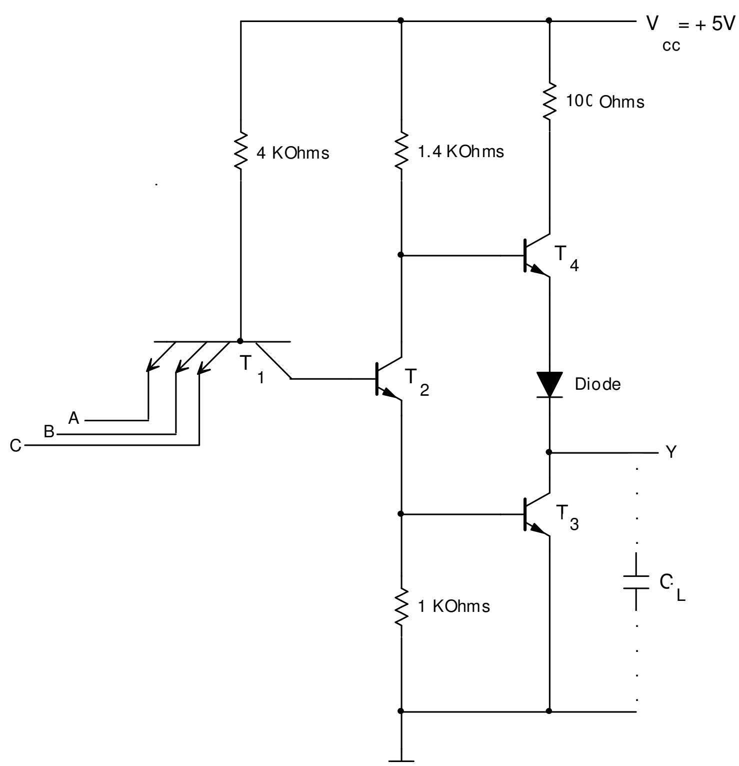


Fig.3(d) Logic Diagram of TTL NAND Gate with Totem Pole Output

Q.26 With the help of a truth table explain the working of a half subtractor. Draw the logic diagram using gates. **(8)**

Ans:

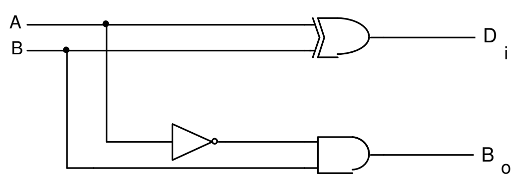
Half Subtractor: A logic circuit for the subtraction of B (subtrahend) from A (minuend) where A and B are 1-bit numbers is referred to as a Half-Subtractor. The truth table for half subtractor is given in Table No.5.1. Here A and B are the two inputs and D_i (difference) and B_o (borrow) are the two outputs. If B is larger than A (e.g., A=0 and B=1), a borrow is necessary,

Inputs		**Outputs**	
A	**B**	**D_i(Difference)**	**B_o(Borrow)**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Table 5.1

From the Truth Table, the logical expressions for D_i and B_o are obtained as

$$D_i = \bar{A}B + A\bar{B}$$
$$B_O = \bar{A}B$$



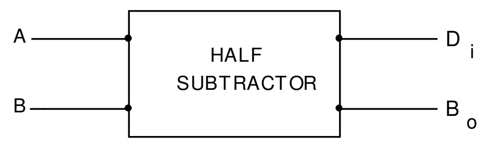


Fig.5(a) Logic Diagram of Half Subtractor **Fig.5(b) Block Diagram of Half Subtractor**

In Table 5.1, input variable *B* is subtracted from A to give output D_i(difference). If B is larger than A *(e.g., A* = 0 and *B* = 1), a borrow is necessary. In the Truth Table, inputs are *A* and *B,* Outputs are D_i (difference) *and* B_O *(borrow).* Hence, the Boolean expressions for the half subtractor from the Truth Table can be written as

$$D_i = A \oplus B \text{ ---------(1)}$$
$$B_O = \bar{A}B \text{ --------(2)}$$

By combining Boolean Expressions (1) & (2), we get the logic circuit for Half Subtractor shown in fig.5(a) and its block diagram is shown in fig.5(b).

Q.27 Draw the logic diagram of a full subtractor using half subtractors and explain its working with the help of a truth table. **(6)**

Ans:

Full Subtractor: A Full Subtractor has to take care of repeated borrow from the next higher bit. At any stage alongwith the two bits (one of which is to be subtracted from the other) is another input B_{in}, i.e., borrow bit from the D_i and borrow B_o. Table shows the truth table.

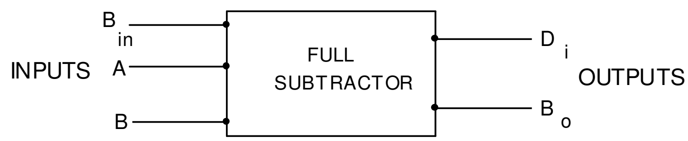


Fig.5(c) Block Diagram of Full Subtractor

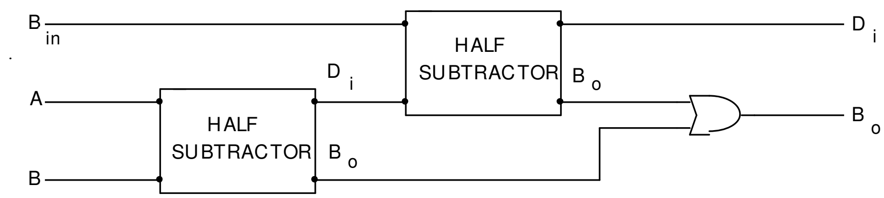


Fig.5(d) Block Diagram of Full Subtractor as Combination of two Half Subtractors and OR Gate

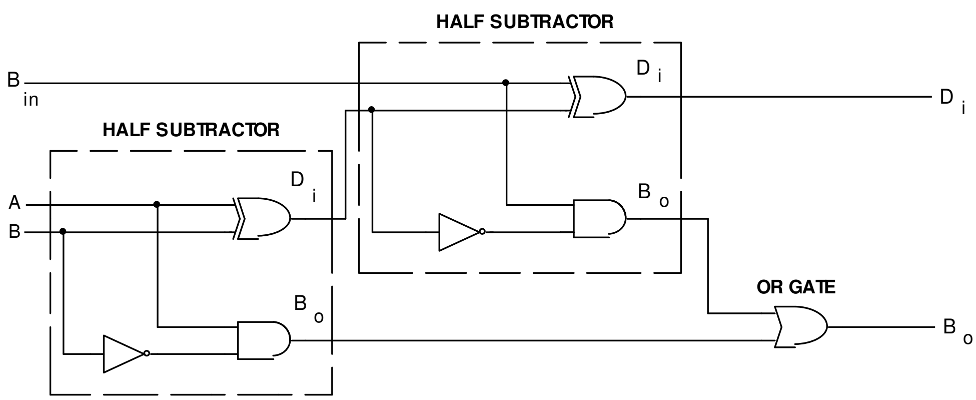


Fig.5(e) Logic Diagram of Full Subtractor

Fig.5(c) shows a block diagram for a full subtractor. It can be constructed from two Half Subtractors and an OR gate as shown in Fig.5(d). The logic diagram is shown in Fig.5(e). This logic diagram is as per the truth table of Table 5.1.

	Inputs		Outputs	
A	**B**	**B_{in}**	**D_i**	**B_O**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 5.1 Truth Table for Full Subtractor

Q.28 Design a BCD to seven segment decoder that accepts a decimal digit in BCS and generates the appropriate output for segments in display indicator.**(14)**

Ans:

BCD-TO-7-Segment Decoder: A digital display that consists of seven LED segments is commonly used to display decimal numerals in digital systems. Most familiar examples are electronic calculators and watches where one 7-segment display device is used for displaying one numeral 0 through 9. For using this display device, the data has to be converted from some binary code to the code required for the display. Usually the binary code used is Natural BCD. Fig.6(a) shows the display device. Fig.6(b) shows the segments which must be illuminated for each of the numerals and Fig.6(c) gives the display system.

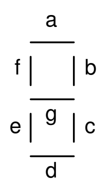


Fig.6(a)

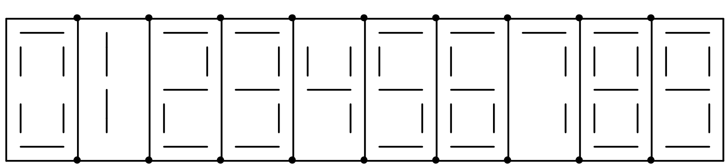


Fig.6(b)

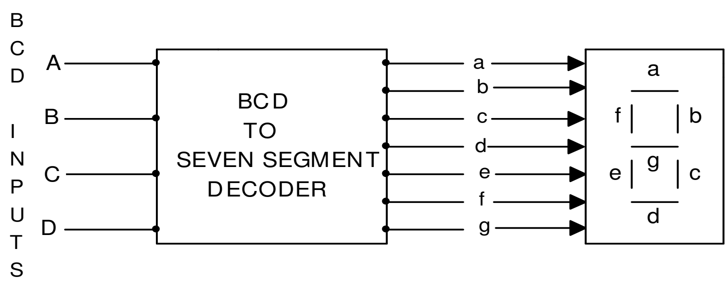


Fig.6(c)

Table 6.1 gives the truth table of BCD-to-7-segment Decoder. Here ABCD is the Natural BCD code for numerals 0 through 9. The K-maps for each of the outputs a through g are given in Fig.6(d), 6(f),6(h),6(j),6(l),6(n),6(p). The entries in the K-map corresponding to six binary combinations not used in the truth table are X –don't care.

Decimal Digit Displayed		**Inputs**						**Outputs**			
	A	**B**	**C**	**D**	**a**	**b**	**c**	**d**	**e**	**f**	**g**
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1

Table 6.1 Truth Table of BCD-to-7 Segment Decoder

(i) K-map and Logic Diagram for Digital Output 'a':

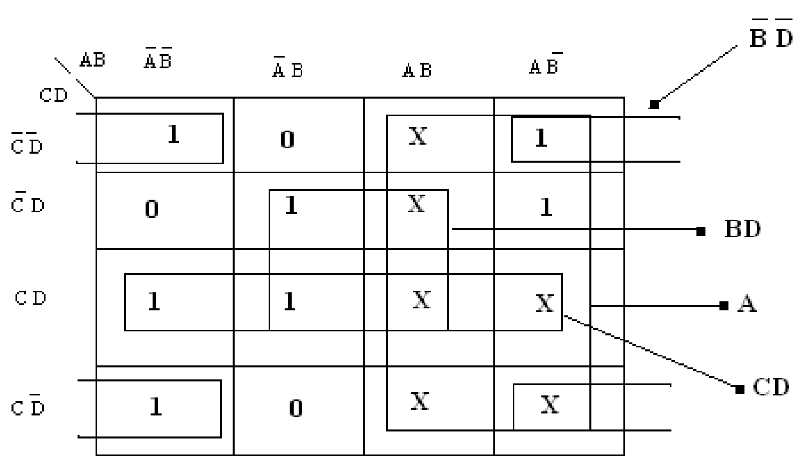


Fig.

6(d) K-map for Output 'a'

The simplified expressions for the Fig.6(d) is given by a = $\bar{B}\,\bar{D}$ + BD + CD + A and the logic diagram is given in Fig.6(e)

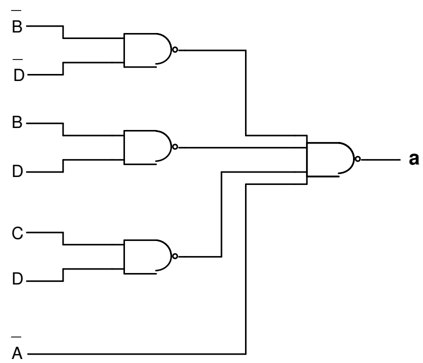


Fig.6(e) Logic Diagram for Output 'a'

(ii) K-map and Logic Diagram for Digital Output 'b':

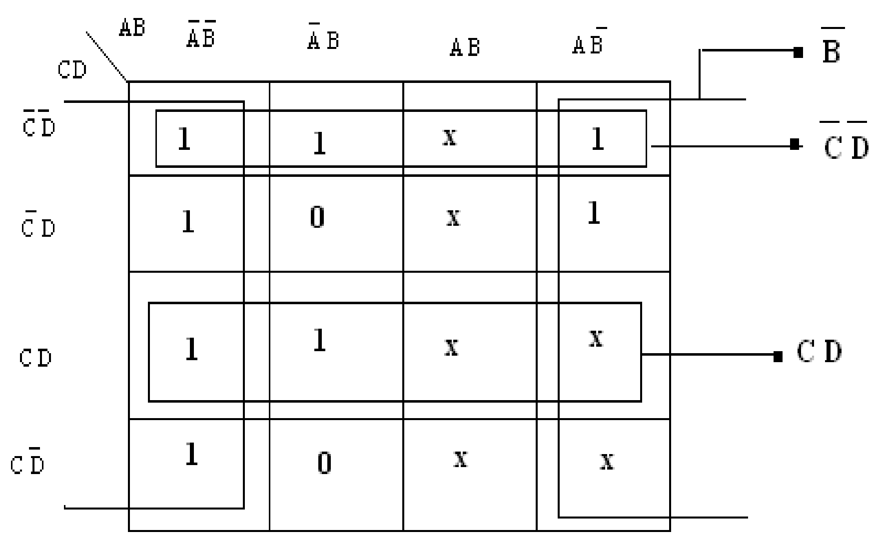


Fig. 6(f) K- map for output 'b'

The simplified expressions for the Fig.6(f) is given by b = $\bar{B} + \bar{C}\,\bar{D}$ + CD and the logic diagram is given in Fig.6(g)

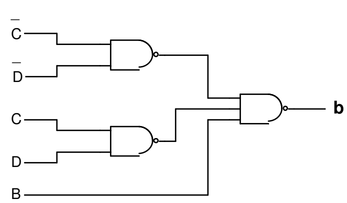


Fig.6(g) Logic Diagram for Output 'b'

(iii) K-map and Logic Diagram for Digital Output 'c':

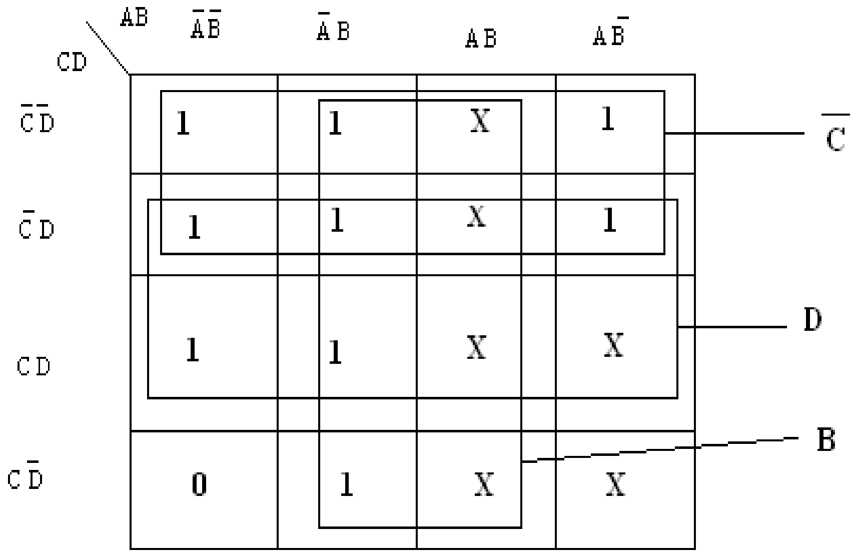


Fig. 6(h) K-map for output `C'

The simplified expressions for the Fig.6(h) is given by c = $B + \overline{C} + D$ and the logic diagram is given in Fig.6(i)

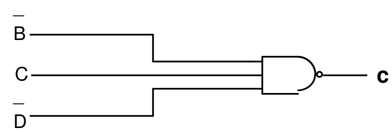


Fig.6(i) Logic Diagram for Output ‘ c ’

(iv) K-map and Logic Diagram for Digital Output‘d’:

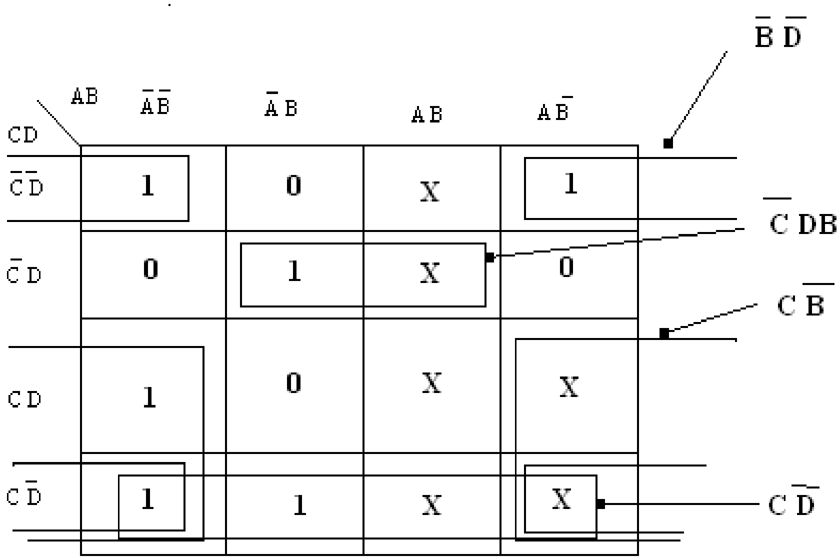


Fig. 6(j) K- map for Output `d'

The simplified expressions for the Fig.6(j) is given by
d = $\overline{B}\,\overline{D} + C\overline{D} + \overline{B}C + B\overline{C}D$ and the logic diagram is given in Fig.6(k)

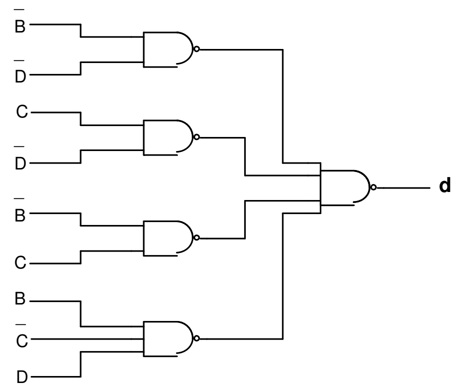


Fig.6(k) Logic Diagram for Output ‘ d ’

(v) K-map and Logic Diagram for Digital Output ‘e’:

CD \ AB	$\overline{A}\,\overline{B}$	$\overline{A}B$	AB	$A\overline{B}$
$\overline{C}\,\overline{D}$	1	0	X	1
$\overline{C}D$	0	0	X	0
CD	0	0	X	X
$C\overline{D}$	1	1	X	X

$\overline{B}\,\overline{D}$, $C\overline{D}$

Fig. 6(l) K-map for output ‘e’

The simplified expressions for the Fig.6(l) is given by e = $\overline{B}\,\overline{D} + C\overline{D}$ and the logic diagram is given in Fig.6(m)

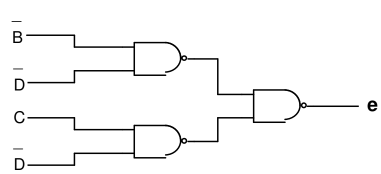


Fig.6(m) Logic Diagram for Output ‘e’

(vi) K-map and Logic Diagram for Digital Output 'f':

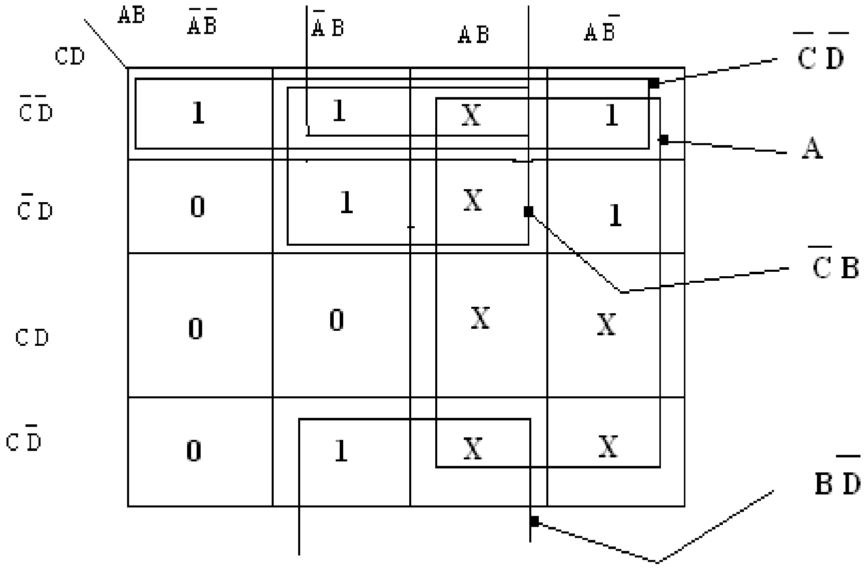


Fig. 6(n) K-map for Output 'f'

The simplified expressions for the Fig.6(n) is given by f = A $+\overline{C}\ \overline{D}$ + B$\overline{C}$ +B$\overline{D}$ and the logic diagram is given in Fig.6(o)

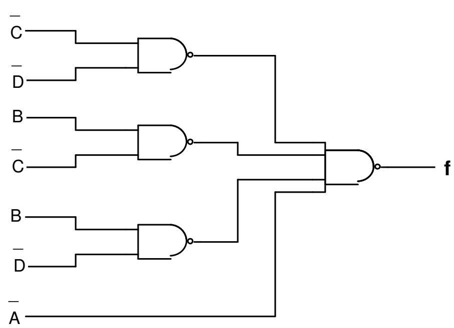


Fig.6(o) Logic Diagram for Output ' f'

(vii)K-map and Logic Diagram for Digital Output 'g':

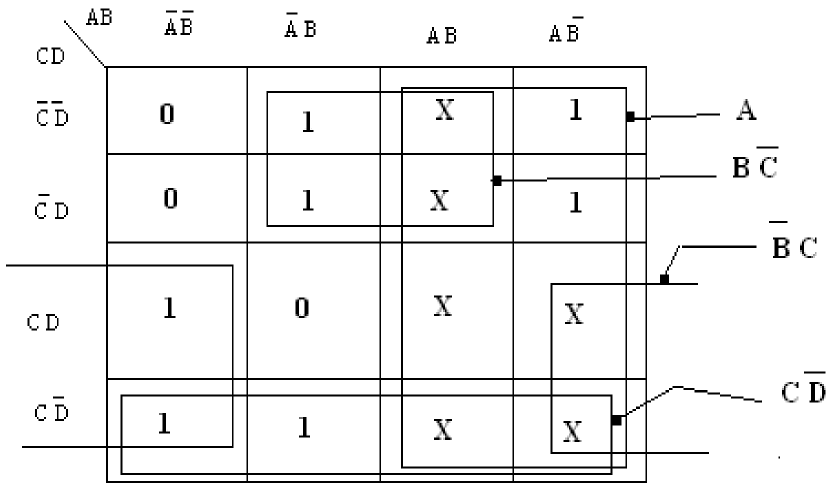


Fig. 6(p) K-map for Output 'g'

The simplified expressions for the Fig.6(p) is given by $g = A + B\ \overline{C} + \overline{B}\ C + C\ \overline{D}$ and the logic diagram is given in fig.6(q).

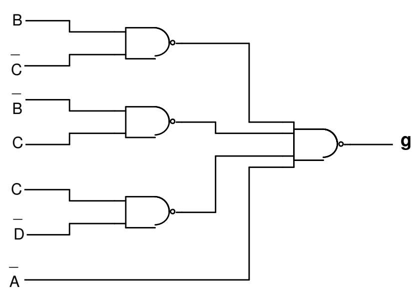


Fig.6(q) Logic Diagram for Output ' g '

Q.29 Explain the working of a demultiplexer with the help of an example. **(6)**

Ans:

1:4 Demultiplexer: Fig.7(a) shows the logic circuit of a 1:4 demultiplexer. It has two NOT gates, 4 AND gates, one data input line, 2 select lines (S_0,S_1) and four output lines *(D_0,* D_1,*D_2,D_3).* The data input line feeds all the AND gates. However, the two select lines enable only one gate at one time. If S_1S_0= 00 then the data goes to D_0. if S_1S_0= 01, then the data goes to*D_1*. If S_1S_0 = 10, then the data goes to D_2 and if S_1S_0= 1, then the data goes to *D_3*.

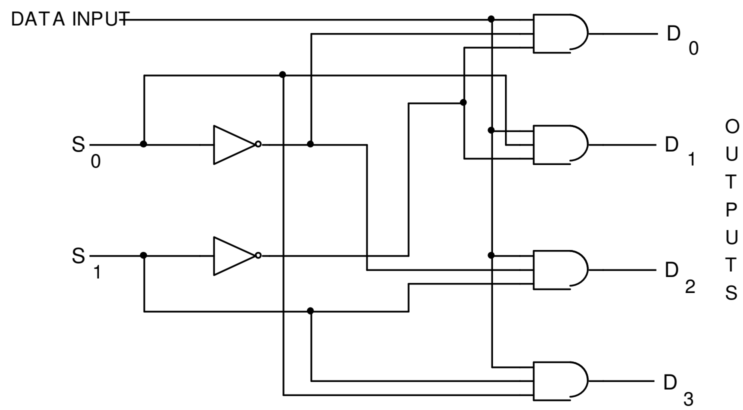


Fig.7(a) Logic Circuit of 1:4 Demultiplexer

Q.30 Give the truth table of S-R and D-flipflops. Convert the given S-R flipflop to a D-flipflop. **(8)**

Ans:

The Truth Table of S-R Flip-Flop is shown in Fig.7(b) and truth table of D Flip-Flop is shown in Fig.7(c)

Inputs		**Output**
S_n	R_n	Q_{n+1}
0	0	Qn
1	0	1
0	1	0
1	1	?

Fig.7(b) Truth Table for S-R Flip-Flop

Input D_n	**Output** Q_{n+1}
0	0
1	1

Fig.7(c) Truth Table for D-Flip-Flop

If we use only the middle two rows of the truth table of the S-R Flip-Flop shown in Fig.7(b) then we obtain a D-type Flip-Flop as shown in Fig.7(d) and 7(e). It has only one input referred to as D-input or Data Input. Its truth table is given in Fig.7(c) from which it is clear that the output Q_{n+1} at the end of the clock pulse equals the input D_n before the clock pulse. This is equivalent to saying that the input data appears at the output at the end of the clock pulse. Thus, the transfer of data from the input to the output is delayed and hence the name Delay (D) Flip-Flop. The D-type Flip-Flop is either used as a Delay Device or as a Latch to store 1-bit of binary information.

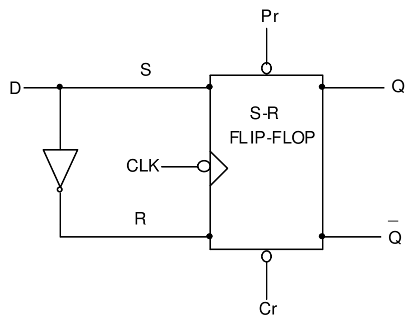


Fig.7 (d) S-R Flip-Flop converted into a D-Flip-Flop

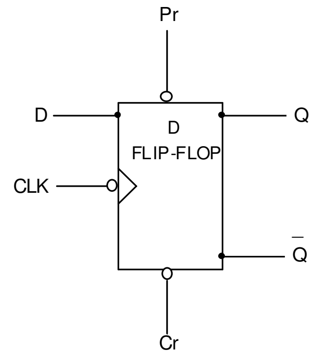


Fig.7 (e) Logic Symbol of D Flip-Flop

Q.31 Define a register. Construct a shift register from S-R flip-flops. Explain its working.**(8)**

Ans:

Register: A register consists of a group of flip-flops and gates that effect their transition. The flip flops hold the binary information and the gates control when and how new information is transformed into the register.

S-R Flip-Flop Shift Register: Shift registers can be built by using SR flip-flops.Fig.9(a) shows the 4-bit shift register, which uses RS flip-flops. It uses Four SR Flip-Flops in cascade and the inputs to the last three flip-flops in the chain receive complementary inputs, that is if S = 0, *R* = 1 and if S = 1, *R* = 0. The first flip-flop has complementary S and *R* inputs and, therefore, it behaves like a D-type flip-flop. Because of the Inverter in the clock line, data will be transferred to flip-flop outputs on the positive going edge of the clock pulse.

There are two inputs *A* and *B*. Any one of the inputs can be used. Since a 1 input at *A* or *B* will be a 1 input at S of the first flip-flop, as a result of double complementation, a positive going clock pulse will produce an output of 1 at Q of the first flip-flop. Normally both *A* and B inputs of the NAND gate are connected together when data is being fed and the NAND is not required to serve as a gate.

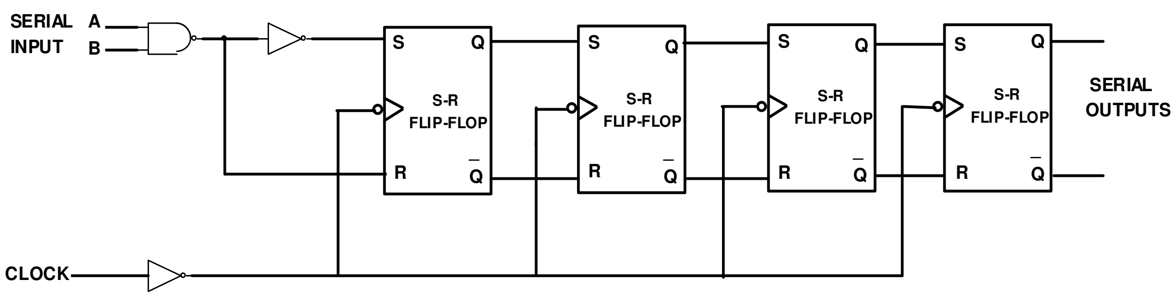


Fig.9(a)Logic Diagram of S-R Flip-Flop Shift Register

Q.32 Explain how a shift register can be used as a ring counter giving the wave forms at the output of the flipflops. **(6)**

Ans:

Shift Register as a Ring Counter: A Ring Counter is a Circular Shift Register with only one flip-flop being set at any particular time; all other are cleared. The single bit is shifted from one flip-flop to the other to produce the sequence of timing signals. Fig.9(b) shows a 4-bit shift register connected as a ring counter. The initial value of the register is 1000, which produces the variable T_0. The single bit is shifted right with every clock pulse and circulates back from T_3 to T_0. Each flip-flop is in the 1 state once every four clock pulses and produces one of the four timing signals shown in Fig.9(c). Each output becomes 1 after the negative-edge transition of a clock pulse and remains 1 during the next clock pulse.

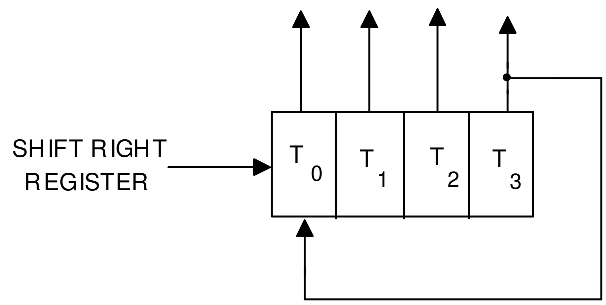


Fig.9(b) 4-bit shift register connected as a ring counter.

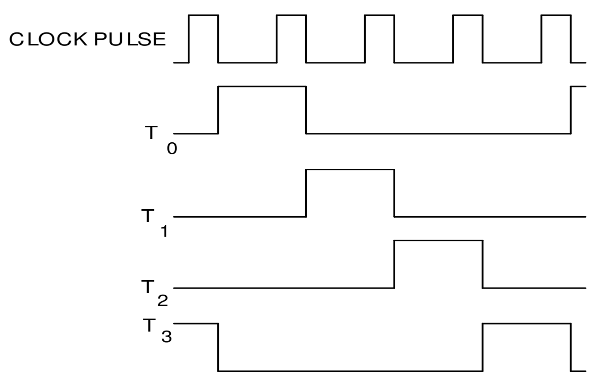


Fig.9(c) Waveforms at the output of Flip-Flops

Q.33 Differentiate between linear addressing and matrix addressing modes with examples. Which of them is the best method? **(4)**

Ans:

Linear Addressing: Addressing is the process of selecting one of the cells in a memory to be written into or to be read from. In order to facilitate selection, memories are generally arranged by placing cells in Linear form or Matrix form.

Linear Addressing Mode: A single column that has n rows and 1 column (such as the 16X1 array of cells) shown in fig.11(a) is frequently called Linear Addressing. Selection of a cell simply means selection of the corresponding row and the column is used.

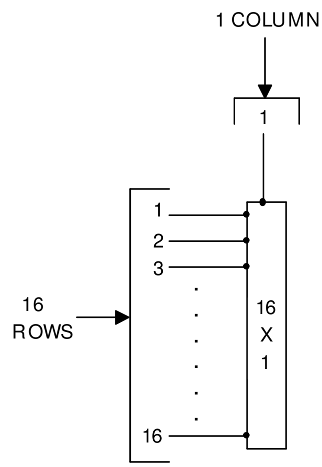


Fig.11 (a) Linear Addressing Mode

Matrix Addressing Mode: The arrangement that requires the fewest address lines is a square array of n rows and n columns for a total memory capacity of n x n = n^2 cells. This arrangement of n rows and n columns is frequently referred to as Matrix Addressing which is shown in fig.11(b).

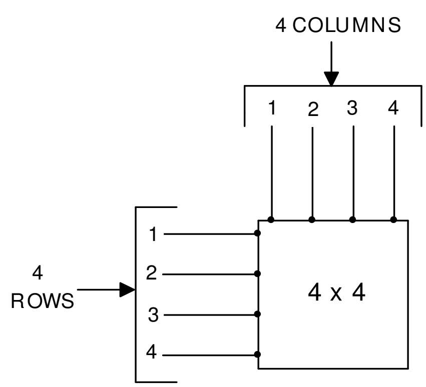


Fig.11(b) Matrix Addressing Mode

Best Method: Matrix Addressing is the best method, because this configuration only requires 8 address lines (i.e.,4 rows and 4 columns), whereas Linear Addressing method requires a total of 17 address lines (i.e., 1 column and 16 rows).The square configuration is so widely used in industry.

Q.34 Write short note on the following: Johnson counter. **(4)**

Ans:

Johnson Counter: Johnson Counter is an synchronous counter, where all flip-flops are clocked simultaneously and the clock pulses drive the clock input of all the flip-flops together so that there is no propagation delay. Fig.11(e) shows the circuit of Johnson counter. In this case the *D* input of FF_0 is driven by $\overline{Q}$ output of FF_3, *i.e.,* the complement of the output of the last flip flop is fed to the *D* of FF_0. This feedback arrangement produces the sequence of states shown in Table 11.2. The 4 bit sequence

has a total of 8 states (n bit sequence will have $2n$ states). Thus an n bit Johnson counter will have a modulus of $2n$.

The Q output of each stage feeds the D input of next stage. But the $\overline{Q}$ output of the last stage feeds the D input of first stage. The counter fills up with 1's from left to right and then fills up 0s again as shown in Table 11.2. Fig. 11*(f)* shows the waveshapes/timing diagram of 4 bit Johnson counter.

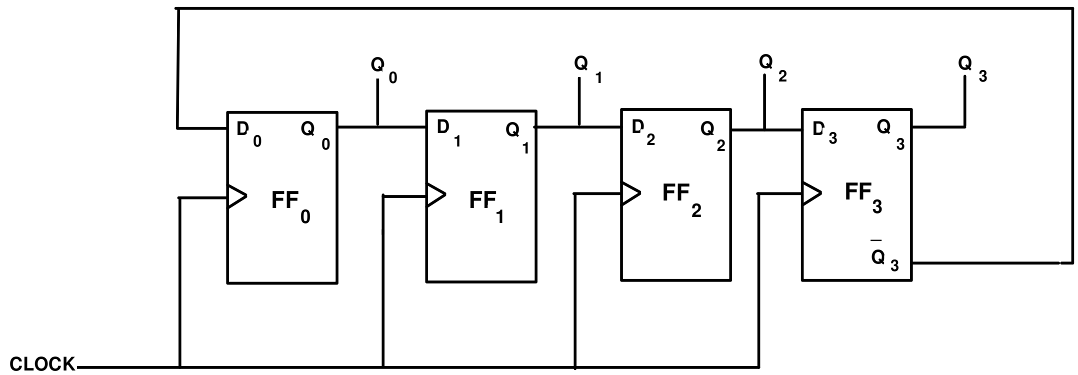


Fig.11(e) Logic Diagram of Johnson counter

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Table 11.2 Sequence of states of 4 bit Johnson Counter

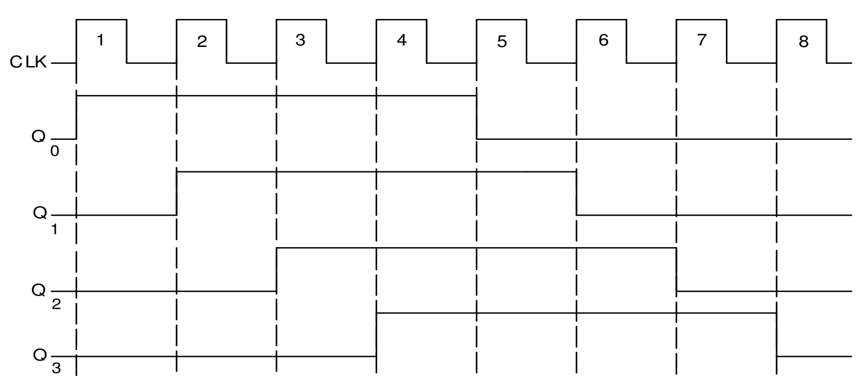
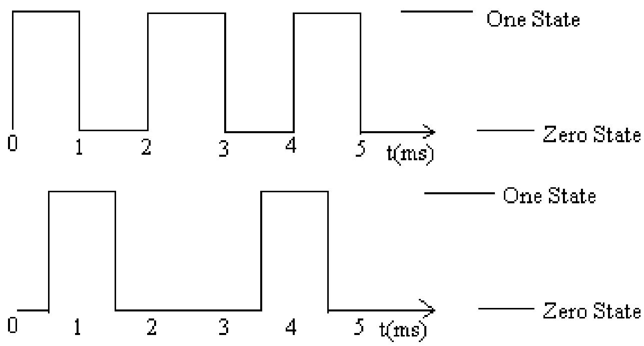


Fig.11(f) Timing Diagram of 4-bit Johnson Counter

Q.35 The voltage waveforms shown in Fig.1 are applied at the inputs of 2-input AND and OR gates. Determine the output waveforms. **(3)**



Ans:

The Output waveforms for AND and OR gates are shown in fig.3(a)

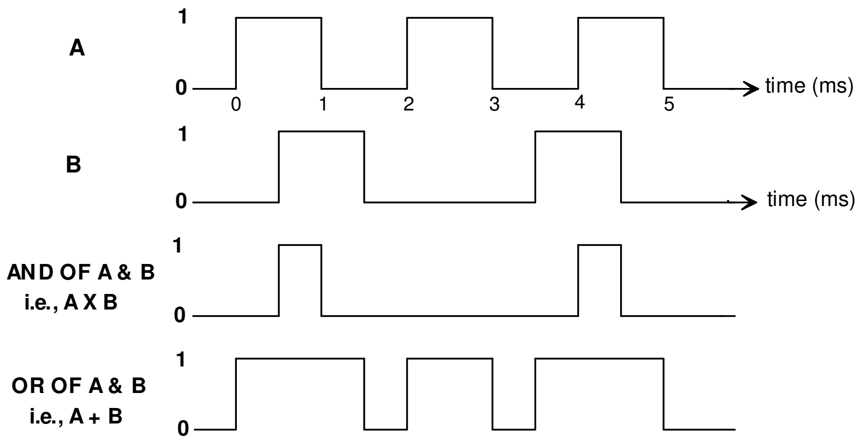


Fig.3(a) Output Waveforms

Q.36 What are the advantages of CMOS logic and explain CMOS Inverter with the help of a neat circuit diagram. **(7)**

Ans:

Advantages of CMOS Logic:

(i) The power dissipation is minimum of all the logic families

(ii) LSI & VLSI are possible

CMOS Inverter:

The basic CMOS logic circuit is an inverter shown in Fig.5(a). For this circuit the logic levels are 0 V (logic 0) and V_{CC} (logic 1). When $V_i = Vcc$, T_1 turns ON and T_2 turns OFF. Therefore $V_O \approx 0$ V and since the transistors are connected in series, the current I_D is very small. On the other hand, when $V_i = 0$ V, T_1 turns OFF and T_2 turns ON giving an output voltage $V_O \approx Vcc$ and I_D is again very small. In either logic state, T_1 or T_2 is OFF and the quiescent power dissipation which is the product of the OFF leakage current and V_{cc} is very low. More complex functions can be realized by combinations of inverters.

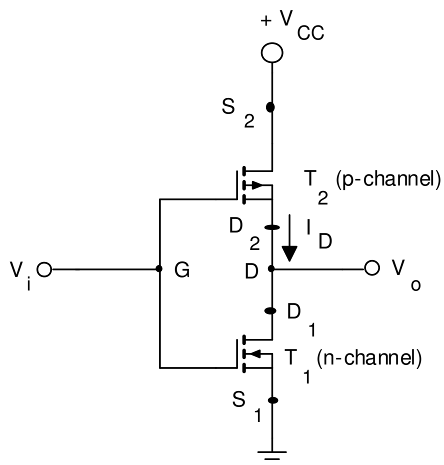


Fig.5(a) Logic Diagram of CMOS Inverter

Q.37 What is Tri-state logic and explain Tri-state logic inverter with the help of a circuit diagram. Give its Truth Table. **(7)**

Ans:

Tri-state Logic:

In normal logic circuits, there are two states of the output, LOW and HIGH. If the output is not in the LOW state, it is definitely in the other state (HIGH). Similarly, if the output is not in the HIGH state, it is definitely in the LOW state. In complex digital systems like microcomputers and microprocessors, a number of gate outputs may be required to be connected to a common line which is referred to as a bus which in turn may be required to drive a number of gate inputs.

When a number of gate outputs are connected to the bus, Totem pole TTL outputs leads to heating of the ICs which may get damaged and Open-collector TTL outputs causes the problems of loading and speed of operation. To overcome these difficulties, in addition to low impedance outputs 0 & 1, there is a third state known as the High-impedance state. Such logic circuits in which the output can have three states is called tri-state logic.

In the Tri-state Logic, in addition to low impedance outputs 0 & 1, there is a third state known as the High-impedance state. When the gate is disabled, it is in the third state.

Tri-state Logic Inverter:

The functional diagram of Tri-state Logic Inverter is shown in fig.5(b) and its logic diagram is shown in fig. 5(c). When the control input is LOW, the drive is removed from T_3 & T_4. Hence both T_3 & T_4 are cut-off and the output is in the third state. When the control input is HIGH, the output Y is Logic 1 or 0 depending on the data input. Truth table of Tri-state Logic Inverter is given in Table No.5.1

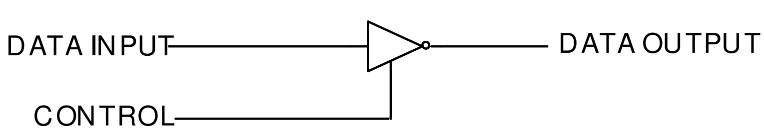


Fig.5(b) Functional Diagram of Tri-state Logic Inverter

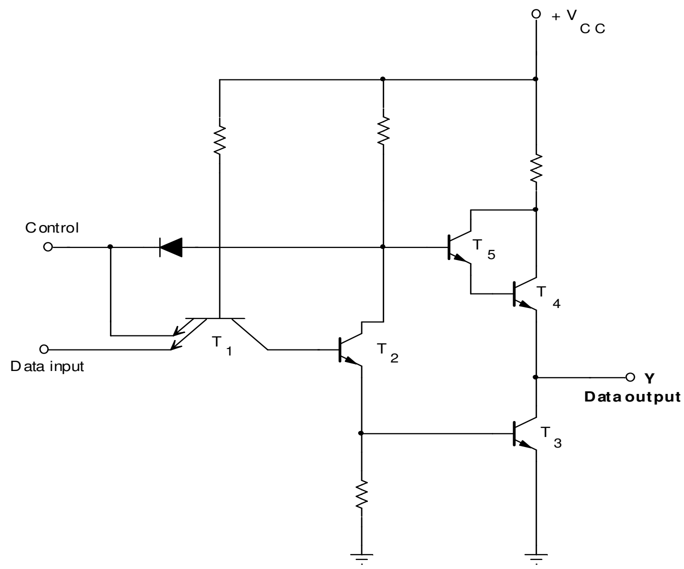


Fig.5(c) Logic Diagram of Tri-state Logic Inverter

Data Input	Control	Data Output
0	0	High - Z
1	0	High - Z
0	1	1
1	1	0

Table 5.1 Truth Table of Tri-state Logic Inverter

Q.38 What is a digital comparator. Explain the working of a 2-bit digital comparator with the help of Truth Table. **(6)**

Ans:

Digital Comparator: The comparison of two numbers is an operation that determines if one number is greater than, less than, or equal to the other number. A Digital comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicate whether A > B, A = B, or A < B.

Comparators can be designed for comparing multibit numbers. Figure 6(e) shows the block diagram of an *n-bit* comparator. It receives two *n-bit* numbers *A* and *B* as inputs and the outputs are *A > B, A = B,* and *A < B.* Depending upon the relative magnitude of the two numbers, one of the outputs will be HIGH. Table 6.2 gives the truth table of a 2-bit comparator.

(I) If the magnitude of the inputs A and B are equal (i.e., A = B): Consider two numbers, A and B as inputs with two digits each i.e., A1, A0 and B1, B0. The two numbers are equal if all pairs of significant digits are equal i.e., if $A_1 = 0, A_0 = 0, B_1 = 0, B_0 = 0$, then $A_1 = B_1$ and $A_0 = B_0$. For example if $A_1 = 0, A_0 = 0, B_1 = 0, B_0 = 0$, then pairs of significant digits i.e., $A_1 = B_1 = 0$ and $A_0 = B_0 = 0$. Output for this combination becomes 1 for A = B and 0 for A < B and A > B. This is given in the Truth Table.

(II) If the magnitude of the input A is greater than or less than B (i.e., A > B or A < B): To determine if A is greater than or less than B, we inspect the relative magnitude of pairs of significant digits starting from the most significant position. If the two digits are equal, we compare the next lower significant pair of digits. This comparison continues until a pair of unequal digits is reached.

(i)If the input A is greater than B (i.e., A > B): If the corresponding digit of A is 1 and that of B is 0, we conclude that A > B. For example if $A_1 = 0$, $A_0 = 1$, $B_1 = 0$, $B_0 = 0$, then pairs of significant digits are $A_1 = B_1 = 0$, and A_0 (i.e., digit 1) > B_0(i.e., digit 0). This is shown in the Truth Table.

(ii) If the input A is less than B (i.e., A < B): If the corresponding digit of A is 0 and that of B is 1, we conclude that A < B. For example if $A_1 = 0$, $A_0 = 0$, $B_1 = 0$, $B_0 = 1$, then pairs of significant digits are $A_1 = B_1 = 0$, and A_0 (i.e., digit 0) < B_0 (i.e., digit 1). This is shown in the Truth Table.

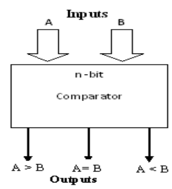


Fig.6(e) Block diagram of n-bit comparator

	Inputs				Outputs	
A_1	A_0	B_1	B_0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Table 6.2 Truth Table of a 2-Bit Comparator

Q.39 What is a Shift Register? What are its various types? List out some applications of Shift Register. **(6)**

Ans:

Shift Register: A register in which data gets shifted towards left or right when clock pulses are applied is known as a Shift Register.

Types of Shift Registers:
(i) Serial-In Serial-Out (SISO) Shift Register
(ii) Serial-In Parallel Out (SIPO) Shift Register
(iii) Parallel-In Serial Out (PISO) Shift Register
(iv) Parallel-In Parallel Out (PIPO) Shift Register

Applications of Shift Registers:
(i) Serial to Parallel Converter
(ii) Parallel to Serial Converter
(iii) Delay line
(iv) Ring Counter
(v) Twisted-ring Counter
(vi) Sequence Generator

Q.40 Design a MOD-6 synchronous counter using J-K Flip-Flops. **(8)**

Ans:

Design of Mod-6 Counter: The Mod-6 synchronous counter, have six counter states (i.e., from 0 to 6). The counter design table for this counter lists the three flip-flop and their states as 0 to 6 and the six inputs for the three flip-flops. The flip-flop inputs required to step up the counter from the present to the next state is worked out with the help of the excitation table. The desired counter states and *the J* K inputs required for counter flip-flops are given in the counter design table shown in Table No.8.1

Input pulse count	Counter States			Flip-Flop Inputs					
	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	X	0	X	0	X
1	1	0	0	X	1	1	X	0	X
2	0	1	0	1	X	X	0	0	X
3	1	1	0	X	1	X	1	1	X
4	0	0	1	1	X	0	X	X	0
5	1	0	1	X	1	0	X	X	1
6(0)	0	0	0						

Table 8.1 counter Design Table for Mod-6 Counter

Flip-Flop A:

The initial state is 0. It changes to 1 after the clock pulse. Therefore, J_A should be 1 and K_A may be 0 or 1 (that is X). In the next state 1 changes to 0 after the clock pulse. Therefore, J_A may be 0 or 1 (i.e., X)and K_A should be 1.

Flip-Flop B:

The initial state is 0 and it remains unchanged after the clock pulse. Therefore, J_B should be 0 and K_B may be 0 or 1 (that is X). In the next state 0 changes to 1 after the clock pulse. Therefore, J_B should be 1 and K_B may be 0 or 1 (i.e., X).

Flip-Flop C:

The initial state is 0 and it remains unchanged after the clock pulse. Therefore J_C should be 0 and K_C may be 0 or 1 (i.e., X). In the next state, it remains unchanged after the clock pulse . Therefore, J_C should be 0 and K_C may be 0 or 1 (i.e., X).The JK inputs required for this have been determined with the help of the excitation table, (Table 8.1). The flip-flop input values are entered in Karnaugh maps shown in Fig. 8b [(i), (ii), (iii), (iv), (v) and (vi)] and a Boolean expression is found for the inputs to the three flip-flops and then each expression is simplified. *As* all the counter states have not been utilized, Xs (don't) are entered to denote un-utilized states. The simplified expressions for each input have been shown under each map. Finally, these minimal expressions for the flip-flop inputs are used to draw a logic diagram for the counter shown in fig.8(c).

A*s* before, the JK inputs required for this have been determined with the help of the excitation table, (Table 8.1). These input values are entered in Karnaugh maps Fig. 8(b)[i to vi] and a Boolean expression is found for the inputs to the three flip-flops and then each expression is simplified. Xs have been entered in those counter states which have not been utilized. The simplified expressions for each input have been shown under each map and finally a logic diagram based on these expressions is drawn and is shown in fig.8(c).

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1	1	X	1
A	X	X	X	X

Map for J_A

$J_A = 1$

Fig.(i)

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	X	X	X	X
A	1	1	X	1

Map for K_A

$K_A = 1$

Fig.(ii)

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	0	0	X	X
A	1	0	X	X

Map for J_B

$J_B = A\overline{C}$

Fig.(iii)

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	X	X	X	0
A	X	X	X	1

Map for K_B

$K_B = A$

Fig.(iv)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	X	X	0
A	0	X	X	1

Map for J_C
$J_C = AB$
Fig.(v)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	0	X	X
A	X	1	X	X

Map for K_C
$K_C = A$
Fig.(vi)

Fig.8(b) Karnaugh Maps for $J_A, K_A, J_B, K_B, J_C, K_C$

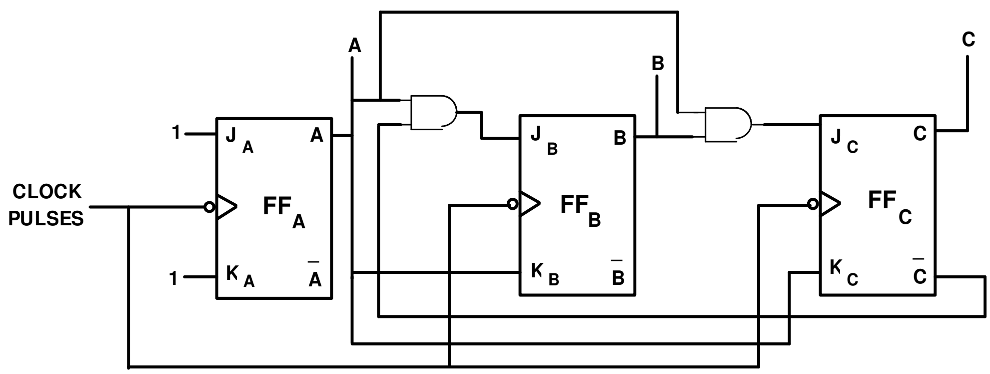


Fig.8(c) Logic Diagram for MOD-6 Synchronous Counter

Q.41 What is ROM? Is the ROM a volatile memory? Explain. **(3)**

Ans:

ROM: Read Only Memory is a Permanent or Semi-permanent Memory. In Permanent ROM, the data is permanently stored and cannot be changed. It can only be read from the memory. There cannot be a write operation because the specified data is programmed into the device by the manufacturer or the user. In Semi-permanent ROM also there is no write operation, but the data can be altered, to a limited extent, by special methods.

No. ROM is a Non-Volatile memory. Programming of ROM involves making of the required interconnections at the time of fabrication and therefore, its contents are unaffected, even when the power is OFF. Thus it is a Non-Volatile Memory.

Q.42 Draw the logic diagram of 16-bit ROM Array and explain its principle of operation. **(8)**

Ans:

16-bit ROM Array: A read-only memory is an array of selectively open and closed unidirectional contacts. .A 16-bit ROM array is shown in Fig. 9(b). To select any one of the 16 bits, a 4-bit address (A_3, A_2, A_1, A_0) is required. The lower order two bits (A1, A_0) are decoded by the decoder D_L which selects one of the four rows, whereas the higher order

two bits (A_3, A_2) are decoded by the decoder D_H which activates one of the four column sense amplifiers.

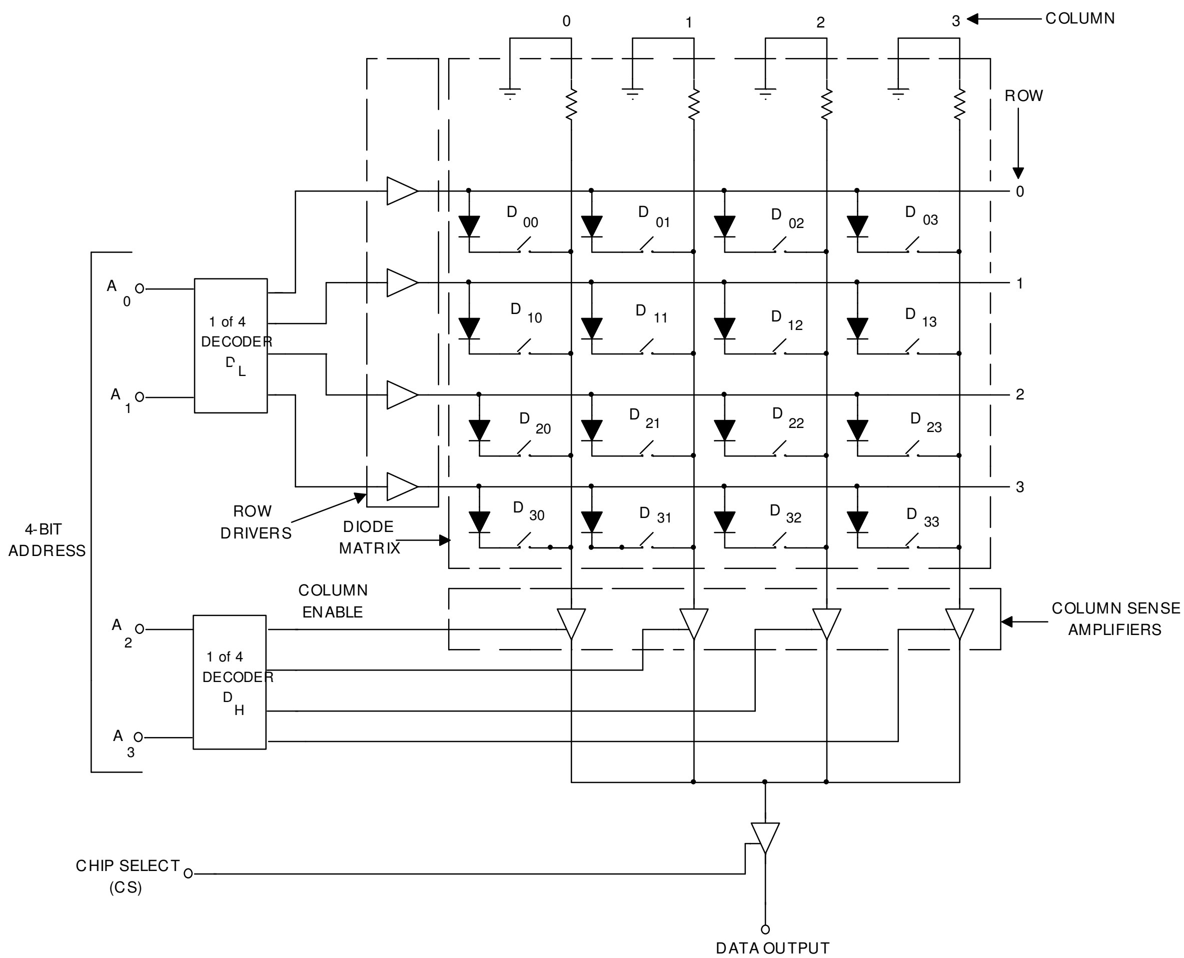


Fig.9(b) Logic Diagram of 16-bit ROM array

The diode matrix is formed by connecting one diode along with a switch between each row and column. For example the diode D_{21} is connected between row 2 and column 1.The output is enabled by applying logic 1 at the chip select *(CS)* input. Programming a ROM means to selectively open and close the switches in series with the diodes. For example, if the switch of diode D_{21} is in closed position and if the address input is 0110, the row 2 is activated connecting it to the column 1. Also the sense amplifier of column 1 is enabled which gives logic 1 output if the chip is selected *(CS* = 1). This shows that a logic1 is stored at the address 0110. On the other hand if the switch of diode D_{21} is open, logic 0 is stored at the address 0110.

Q.43 Explain briefly, why dynamic RAMs require refreshing? **(3)**

Ans:

Because of the charge's natural tendency to distribute itself into a lower energy-state configuration (i.e., the charge stored on capacitors leak-off with time), dynamic RAMs require periodic charge refreshing to maintain data storage.

Q.44 Draw the schematic circuit of an Analog to Digital converter using Voltage-to Frequency conversion and explain its principle of operation. Draw its relevant Waveforms. **(10)**

Ans:

Analog to Digital Converter Using Voltage-to-Frequency Conversion:An analog voltage can be converted into digital form by producing pulses whose frequency is proportional to the analog voltage. These pulses are counted by a counter for a fixed duration and the reading of the counter will be proportional to the frequency of the pulses and hence to the analog voltage.

A voltage-to-frequency converter is shown in Fig. 10(a). The analog voltage V_a is applied to an integrator whose output is applied at the inverting input terminal of a comparator. The non-inverting input terminal of the comparator is connected to a reference voltage $-V_R$. Initially, the switch S is open and the voltage v_o decreases linearly with time ($v_o = V_a t/\tau$) which is shown in Fig. 10(b). When the decreasing v_o reaches $-V_R$ at $t = T$, the comparator output V_C goes HIGH. This is used to close the switch S through a monostable multivibrator. When the switch S is closed, the capacitor C discharges, thereby returning the integrator output v_o to 0. Since the pulse width of the waveform V_C is very small, therefore, a monostable multivibrator is used to keep the switch S closed for a sufficient time to discharge the capacitor completely. The rate at which the capacitor discharges depends upon the resistance of the switch.

Let the pulse width of the monostable multivibrator be T_d. Therefore, the switch S remains closed for T_d after which it opens and v_o starts decreasing again.

If the integration time $T >> T_d$, the frequency of the waveforms v_o and V_C is given by

$$f = \frac{1}{T + T_d} \cong \frac{1}{T} = \frac{1}{\tau}\frac{V_a}{V_R}$$

Thus we obtain an output waveform whose frequency is proportional to the analog input voltage. An *A/D* converter using the voltage-to-frequency *(V/F)* converter is shown in Fig. 10(c). The output of the *V/F* converter is applied at the clock *(CK)* input of a counter through an AND gate. The AND gate is enabled for a fixed time interval T_1. The reading of the counter at $t = T_1$ is given by

$$n = fT_1 = \frac{1}{\tau}\frac{V_a}{V_R}T_1 \text{ which is proportional to } V_a.$$

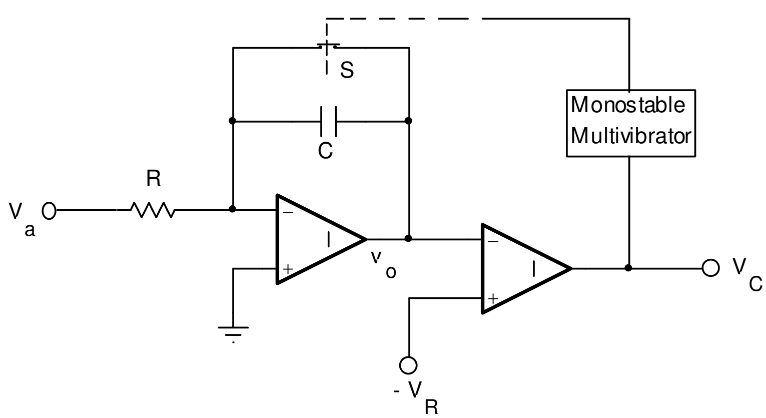


Fig.10(a) Logic diagram of Voltage-to-Frequency Converter

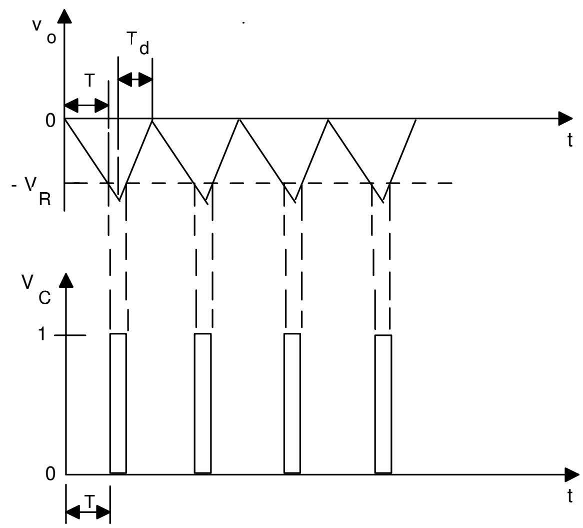


Fig.10(b) Waveforms of Voltage-to-Frequency Converter

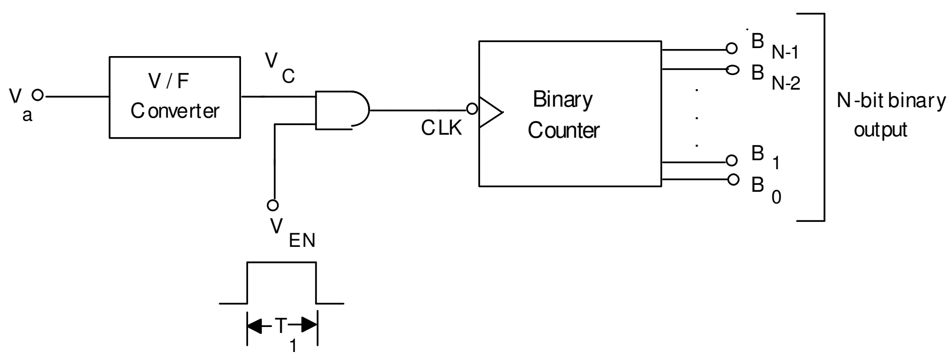


Fig.10(c) Schematic circuit of A/D converter using a V/F converter

Q.45 With the help of R-2R binary network, explain the working of a 3-bit D/A converter and derive an expression for the output voltage. **(10)**

Ans:

R-2R ladder D/A converter: An *R-2R* ladder D/A converter is shown in Fig.11(a). It uses resistors of only two values R and *2R.* The inputs to the resistor network are applied through digitally controlled switches. A switch is in 0 or 1 position corresponding to the digital input for that bit position being 0 or 1 respectively. Now, we consider a 3-bit *R-2R* ladder *D/A* network shown in Fig.11(b).In this circuit we have assumed that the digital input as 001.

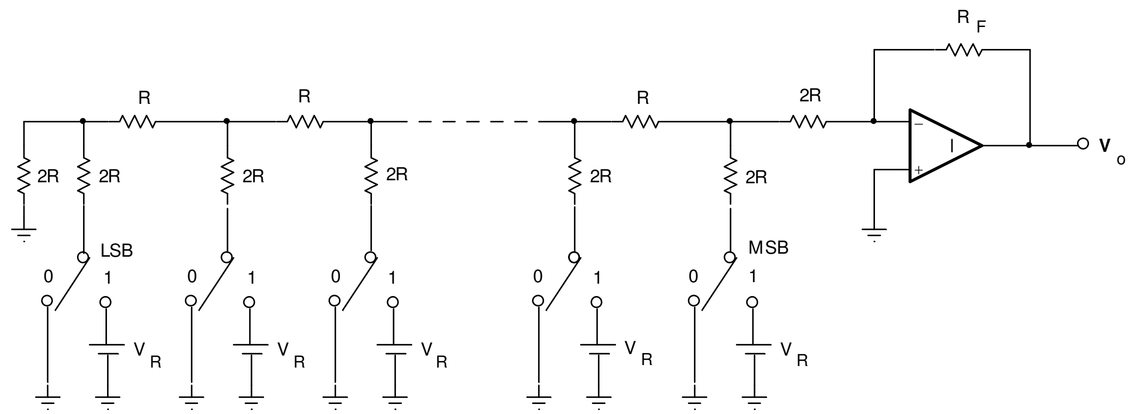


Fig.11(a) Logic Diagram of R-2R Ladder D/A Converter

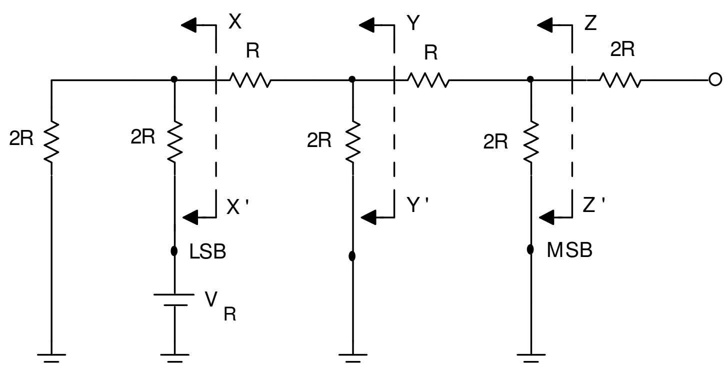


Fig.11(b) 3 bit R-2R Ladder D/A Network

The circuit is simplified using Thevenin's theorem. Applying Thevenin's theorem at *XX'*, we obtain the circuit of Fig. I1(c). Similarly, applying Thevenin's theorem at *YY'* and *ZZ'*, we obtain the circuits of Fig.11(d) and 11(e) respectively. Here, LSB is assumed as 1 and the equivalent voltage obtained is $V_R / 2^3$.

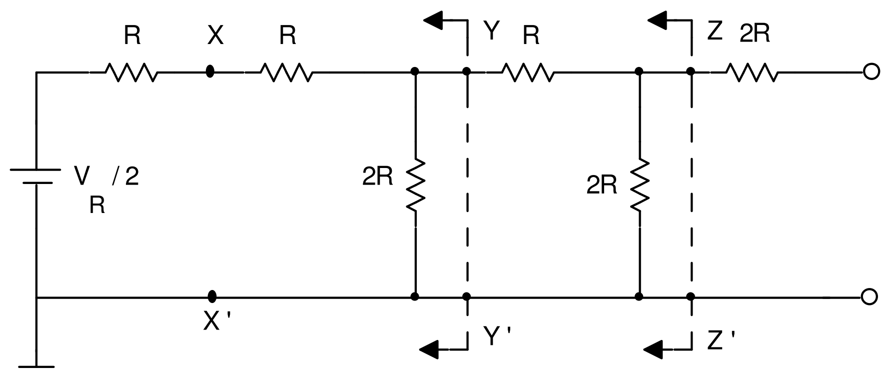


Fig.11(c) Equivalent circuit after applying Thevenin's Theorem at XX'

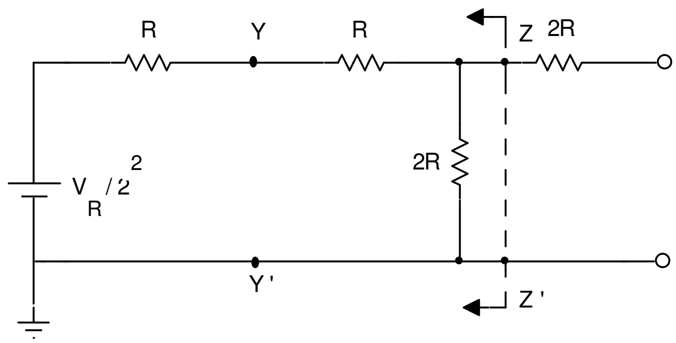


Fig.11(d) Equivalent circuit after applying Thevenin's Theorem at YY'

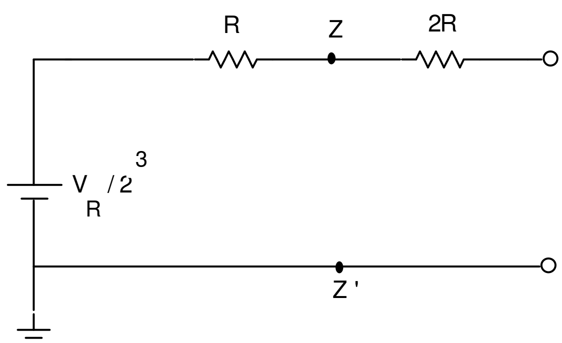


Fig.11(e) Equivalent circuit after applying Thevenin's Theorem at ZZ'

Similarly for the digital input of 010 and 100 the equivalent voltages are $V_R/2^2$ and $V_R/2^1$ respectively. The value of the equivalent resistance is 3R in each case. Therefore, we obtain an equivalent circuit of 3-bit R-2R Ladder D/A Converter which is given in Fig.11(f). The output analog voltage V_O is given by

$$V_O = -\left(\frac{R_F}{3R} . \frac{V_R}{2^3} b_0 + \frac{R_F}{3R} . \frac{V_R}{2^2} b_1 + \frac{R_F}{3R} . \frac{V_R}{2^1} b_2 \right)$$

$$V_O = -\left(\frac{R_F}{3R} \right) . \left(\frac{V_R}{2^3} \right) [4b_2 + 2b_1 + 1b_0]$$

Hence the above equation shows that the analog output voltage is proportional to the digital input.

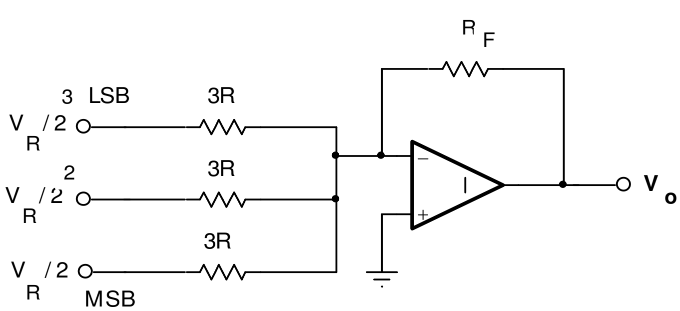


Fig.11(f) Equivalent circuit of 3-bit R-2R Ladder D/A Converter

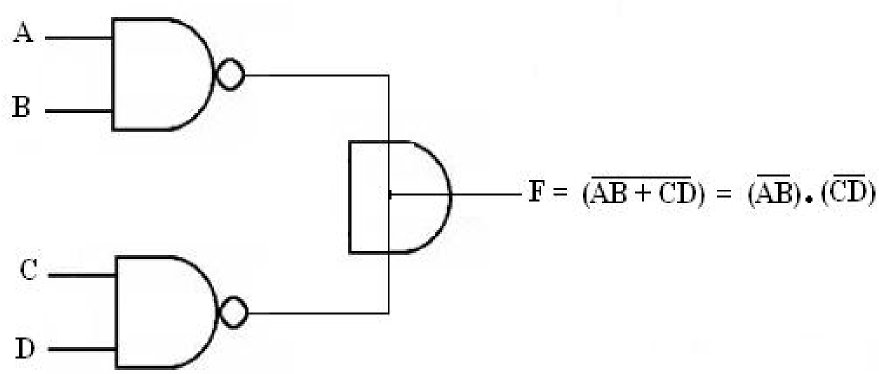
Q.46 What is meant by Wired-AND connection of digital ICs? What are its advantages and disadvantages? Draw a circuit of TTL gates with Wired-AND connection and explain its operation. **(10)**

Ans:

Wired AND digital IC: If input F and F' at two DTL NAND gates connected, the output can be considered as AND operations between the logic output. Because when both the output corresponds to cut-off stages of the transistors, the output will be unaffected and logic 1.when any of the outputs corresponds to the saturation condition approx 0.2 volt, the output from common point will become 0.2 volt. If A and B both input are DTL NAND gate and the C,D, are input for another ,NAND the output Y on joining F and F' at common terminal as follows: Y=(A.B)'.(C.D)'=(A.B+C.D)'

Wired – AND Connection

In digital IC`s NAND and NOR gates are most often used. For this reason NAND and NOR logic implementation are the most important from the practical point of view, some NAND & NOR gates are realized using wire connections between the o/p`s of two gates to provide a specific logic function. This type of logic is called as wired logic.



Wired – AND in open collector TTL gates

Advantages and disadvantages

- In this IC additional logic is performed without additional hardware.
- There is an effective reduction in the fan out of the gate.
- In the wired- AND connection speed of operation increases.
- Power dissipation in low output state in P(O) increases because of reduction in effective collector resistor.
- Current dissipation in logic 0 state will increases when two TTL gates with passive pull ups are ANDed by wired logic.
- The TTL fates with missing pull up circuit at the collector are also called open collector gates. These are more suitable for the wired connections.

Q.47 What is the necessity of Interfacing in digital ICs and what are the points to be kept in view, while interfacing between TTL gate and CMOS gate? **(4)**

Ans:

To achieve the optimum performance in digital system, device from more than one logic families can be used ,which takes advantages of the superior characteristics of each logic families. For example, CMOS logic ICs can be used in those parts of the system where low power dissipation is required, and TTL can be used where high speed of operation is required. When CMOS derives TTL, the following conditions are required to be satisfied.

$V_{OH(CMOS)} \geq V_{IH(TTL)}$

$V_{OL(CMOS)} \leq V_{IL(TTL)}$

$-I_{OH(CMOS)} \geq NI_{IH(TTL)}$

$-I_{OH(CMOS)} \geq -NI_{IL(TTL)}$

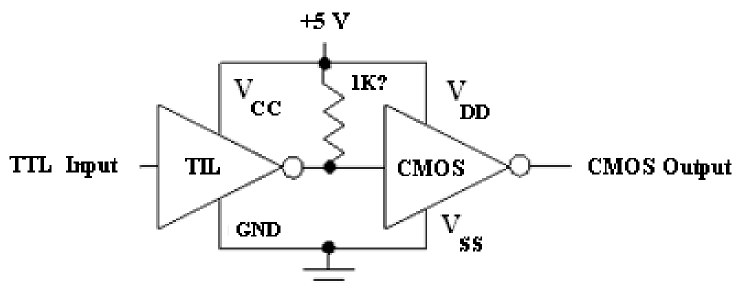


Figure 1: TTL-to-CMOS interfacing using pull-up register.

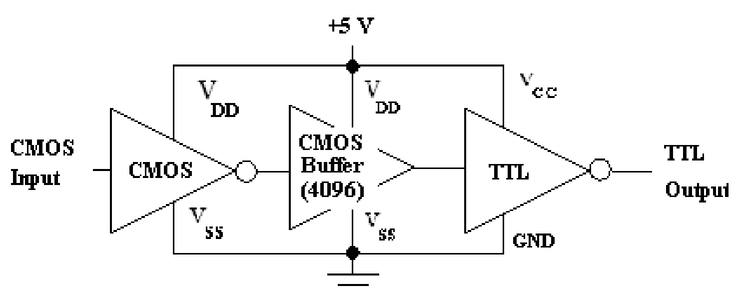
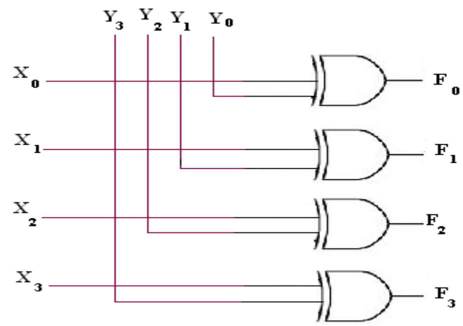


Figure 2: CMOS-to-TTL interfacing using a CMOS buffer IC

Q.48 Draw the logic diagram of 4-bit odd parity checker using EX-NOR gates and explain its operation with the help of Truth table. **(7)**

Ans:

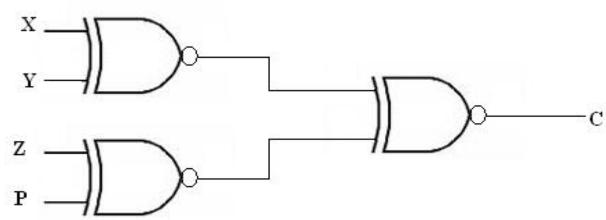
4 bit odd parity checker using XNOR circuit:-The concept of parity checker ,Wherein the additional bit is known as parity. It can be either even or odd. The following circuit will give the 4 bit parity checker circuit.



logic diagram of 4-bit odd parity checker using EX-NOR gates

Parity checker networks are logic circuits with exclusive – OR functions. Ex OR operation of parity bit is a scheme for detecting errors during transmission of binary information. It is an extra bit transmitted and then checked at the receiving end for errors.

In 4 bit odd parity checker, the three bits X,Y,Z constitute the message and `P` is the parity bit. For odd parity bit `P` is generated, so as to make the total number of 1`s odd (including P). The three bit message and the parity bit are transmitted to their destination; they are applied to a parity checker circuit. An error occurs during transmission if the parity of the four bits received is even, since binary information transmitted was originally odd. The output "C" of the parity checker should be "1"when an error occurs i.e. when the number of 1's in the four input is even.



4 BIT odd Parity checker

Truth Table

Four bits received				Parity error check
x	y	z	P	C
0	0	0	0	------------- 1
0	0	0	1	------------- 0
0	0	1	0	------------- 0
0	0	1	1	------------- 1
0	1	0	0	------------- 0
0	1	0	1	------------- 1
0	1	1	0	------------- 1
0	1	1	1	------------- 0
1	0	0	0	------------- 0
1	0	0	1	------------- 1
1	0	1	0	------------- 1
1	0	1	1	------------- 0
1	1	0	0	------------- 1
1	1	0	1	------------- 0
1	1	1	0	------------- 0
1	1	1	1	------------- 1

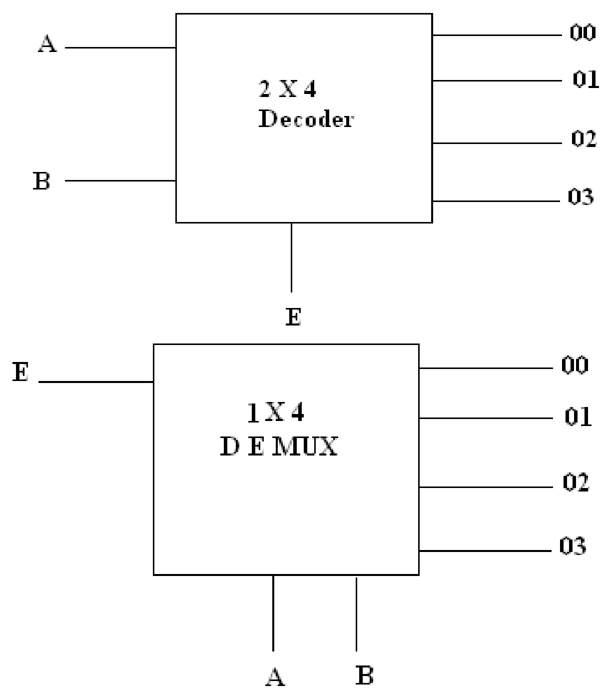
Q.49 What is a Decoder? Compare a decoder and a demultiplexer with suitable block diagrams. **(4)**

Ans:

Decoder:- It decodes the information. The decoders have n inputs 7 at the end maximum 2^n outputs because n bit no can decode max 2^n information , Now 1 enable input 'E ' is connected to the decoder. If it is high then only the circuit will be enabled and it will work as a decoder. If 'E' is low then the circuit will be disabled.

Demultiplexer has the same circuit as decoder but here e is taken as the single input line, the output lines are same as decoder (i.e max 2^n). The information at E will be transmitted to one of the output line and the output line will be selected by bit combination of n select lines.

Block diagrams of a decoder and a demultiplexer

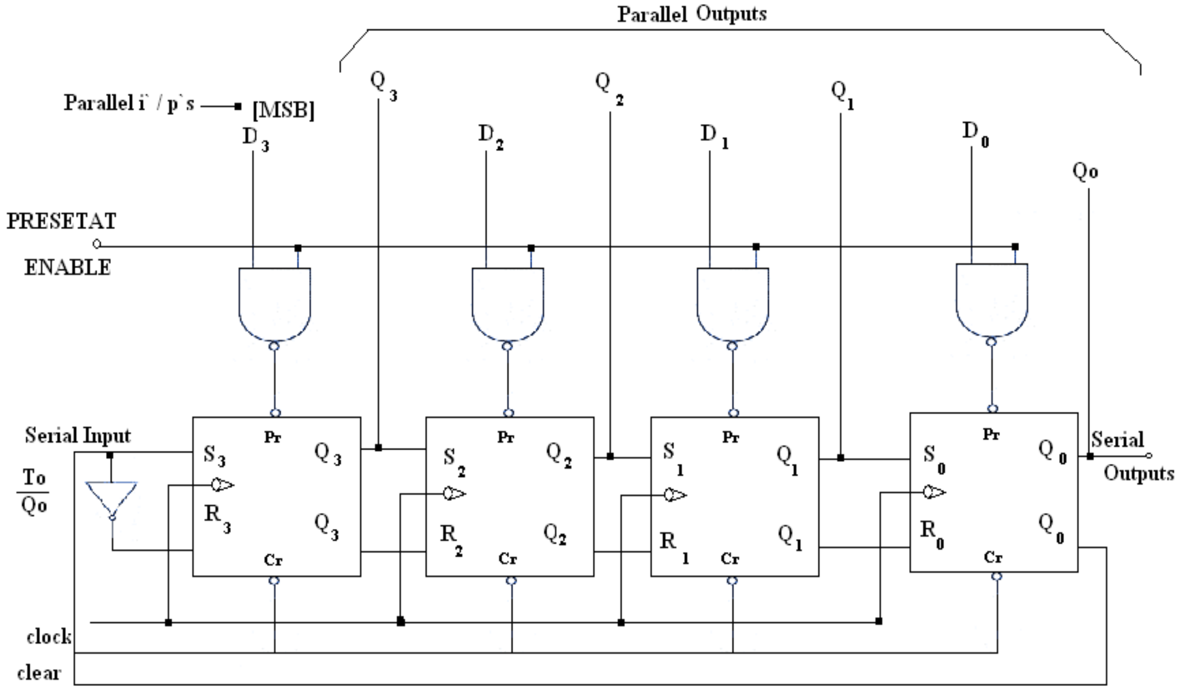


Q.50 Draw the logic diagram of 4-bit Twisted Ring counter and explain its operation with the help of timing diagram. **(6)**

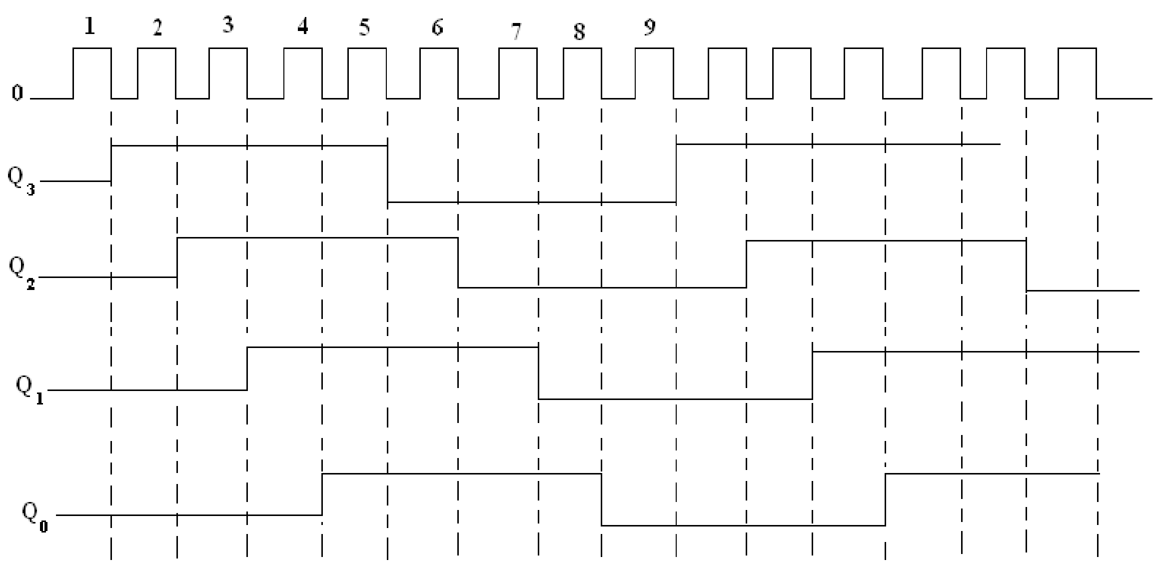
Ans:

Twisted ring counter (4 BIT) We know that shift registers can operate in 4 different modes that is SISO, SIPO, PISO and PIPO.

Following is the 4 BIT register which can operate in any of the mode. If $\overline{Q}_0$ is applied to the serial input , the resulting circuit is called twisted ring or Johnson Counter. If the clock pulse are applied after clearing the Flip Flops, square wave form is obtained at the Q output.

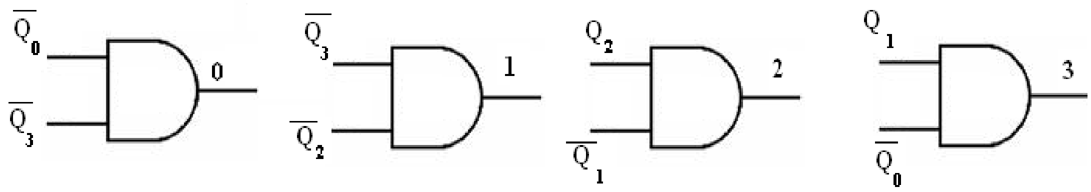


The logic diagram of 4-bit Twisted Ring counter



Wave form of u bit Twisted Ring Counter

For decoding the count, two input AND Gates are required Decoding logic for 4 stage twisted ring counter are



Q.51 Explain the following characteristics for digital IC's. **(8)**
(i) Propagation delay (ii) Power dissipation

Ans:

Propagation Delay:- The speed of operation of a digital IC is specified in terms of propagation delay time. The delay time is measured between the 50% voltage levels of input & output wave forms. There are two delay times.

a) t_{phl} = When the O/P goes from HIGH state to LOW state.
b) t_{plh} = When the O/P goes from Low state to HIGH state.

The propagation delay time of the logic gate is taken as the average of these two delay times.

Power Dissipation:- This is amount of power dissipated in an IC. It is determined by the current I_{CC} , that it draws from the V_{cc} supply and is given by V_{CC} X I_{CC}. This is specified in milliwatts. I_{cc} is the average value of I_{cc} (o) and I_{cc} (1)

Q.52 How will you form an 8 bit adder using 2 four bit adder IC's 7483? **(8)**

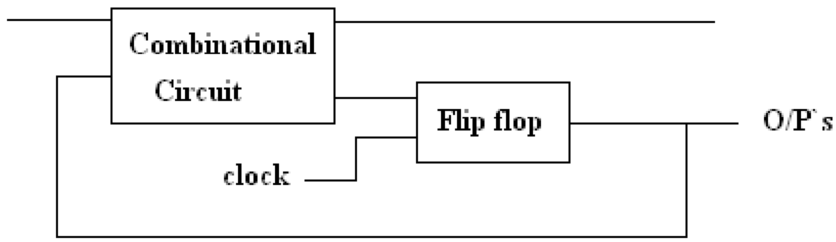
Ans:
IC 7483 is a 4 bit adder IC. It has two four bit data inputs and output carry, 4 bit data output carry. These two IC's should be connected in cascade, the first IC will add lower order bits and it generate sum and carry. This carry should be the input of second IC, The inputs of second IC will be the higher order bits of number A & B

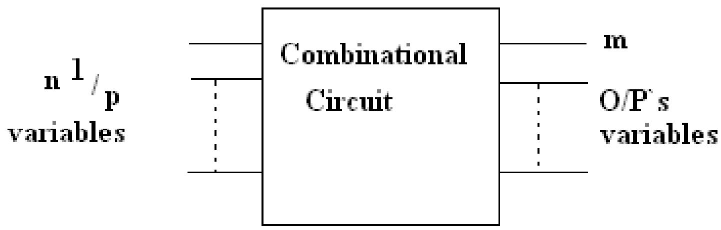
Q.53 Distinguish between combinational logic circuits and sequential logic circuits. How are the design requirements of combinational circuits specified? **(7)**

Ans:
Combinational logic circuits:-
(i) Outputs only depends upon present state of the input.
(ii) No memory element present or no feedback connection.

Sequential logic circuit:-
(i) Output not only depends on the present state of the input but also depend on the previous state of the output.
(ii) Memory element is present or a feedback connection is there.

Block diagram of Sequential circuit





Block diagram of Combinational circuit

Design Requirements of Combinational Logic:-

(i) From the specifications of circuit, we determine the no of inputs & outputs.

(ii) Derive the truth table which contains all possible combination of the inputs and corresponding outputs.

(iii) Minimize the output function using K-Map.

(iv) Draw the logic diagram.

Design Requirements of Sequential circuit:

(i) The circuit specifications translated into a state diagram.

(ii) The state diagram is then converted into state table.

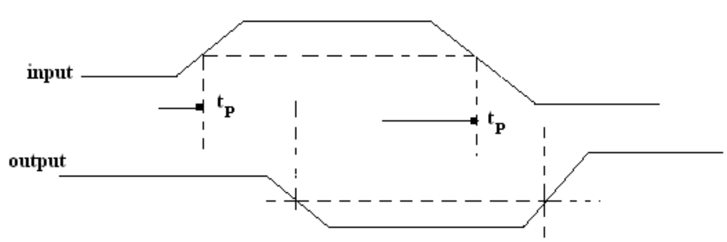
(iii) From state table, information for obtaining logic circuit diagram is obtained.

Q.54 What are the characteristics of digital ICs used to compute their performance? **(11)**

Ans:

<u>**Characteristics of Digital Integrated Circuits**</u>

1. **Speed of operation:** The Speed of a digital circuit is specified in terms of the propagation delay time. The input and output delay times can be shown as:



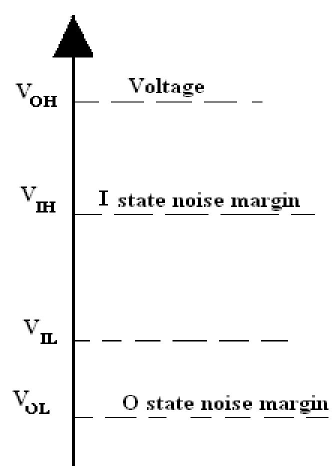
The delay times are measured between the 50 percent voltage levels of input and output wave forms. There are two delay times t_{phl}, when the O/P goes from the high state to low state and t_{phl}, when O/P goes from low state to high state.

2 **Power Dissipation:** This is the amount of power dissipated in an IC. It is determined by the current, I_{CC} that it draws from the V_{cc} supply and is given by V_{cc} X I_{cc}. I_{cc} is the av value of I_{CC} [O] and I_{cc} [1]. It is specified in mW.

3 **Figure of merit:** For digital IC, it is defined as the product of speed and power. It is specified in Pico joules [as ns x mw= pj]. A low value of speed power product is desirable.

4 **Fan Out:** This is the no of similar gates which can be driven by a gate. High fan out is advantageous, as it reduces the need for additional drivers to drive more gates.

5 **Noise Immunity:** Stray electric and magnetic fields induce unwanted voltages known as noise, on the connecting wires between logic circuits. This may cause the voltage at the I/P to a logic circuit to drop below V_{ih} or fuse above V_{il} and may produce undesired operation. The circuit`s ability to tolerate noise signals is referred to as the noise immunity.



6. **Operating Temperature:** The temperature range in which an IC functions properly must be known. The accepted temperature range for consimer IC` s are 0 to 70 degree C and for industrial applications [-55° C to +125° C for military applications].

Q.55 What is a digital multiplexer? Illustrate its functional diagram. Write the scheme of a 4-input multiplexer using basic gates (AND/OR/NOT) and explain its operation. **(8)**

Ans:

Multiplexer: MUX or data selector is a logic circuit selects binary information from one of many input and directs it to a single output line. Selection of the particular input line is controlled by a set of selection lines. Normally there are 2^n input lines and correspondingly n selection lines.

There are 4 inputs I_1 I_0 I_2 I_3 and two selection line S_0 and S_1. Depending upon the bit combination of S_0 and S_1 one of the input is transferred to the output. Basically there is a decoder circuit with one input for each bit of information and one OR gate connected to

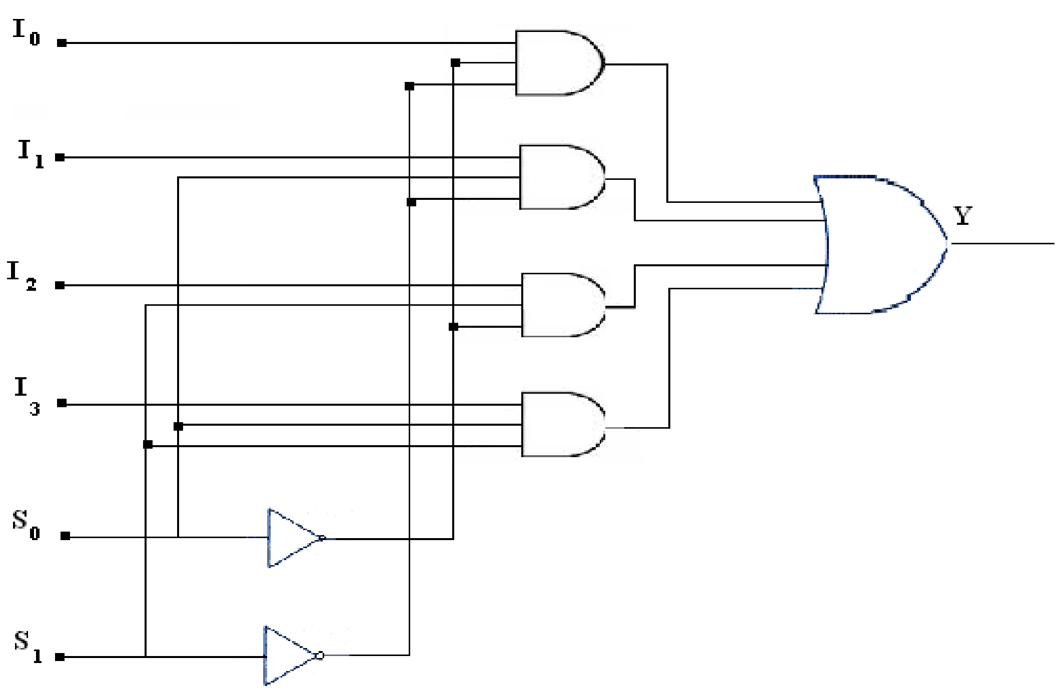
the output. If S_o, S_i = 00 ,then first AND gate will have the two inputs as one output will depend on I_0. At the same time outputs of all other AND gates are Zero.
The multiplexer is a combinational circuit which is one of the most widely used standard circuit in digital design. It has N select lines 2^N inputs and a single output.

Multiplexer:-

$$Y = \bar{S}_1\bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$$

Truth table of 4x1 Mux

Select inputs		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

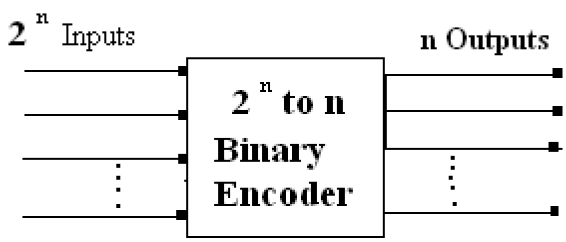


Circuit Diagram of 4 X 1 MUX using basic gate

Q.56 What is meant by a priority encoder? Name the 7400 series TTL chip which is a priority encoder. Write its truth table. Illustrate how it can be used as a decimal-to-BCD encoder. **(8)**

Ans:

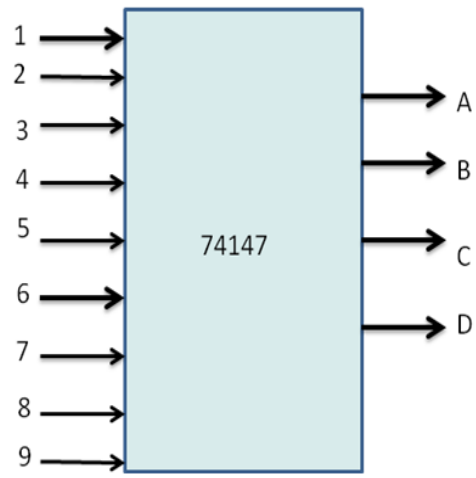
Priority encoder- An encoder is a combinational circuit that performs the inverse operation of a decoder. If a device output code has fewer bits than the input code has, the device is usually called an encoder. e.g. 2^n-to-n, priority encoders. The simplest encoder is a 2^n-to-n binary encoder, where it has only one of 2^n inputs = 1 and the output is the n-bit binary number corresponding to the active input.



One of the most commonly used input device for a digital system is a set of 10 switches, one for each numeral between 0 & 9. These switches generate 1 or 0 logic levels in response to turning them off or on. When a particular number is to be fed to the digital circuit in BCD code, the switch corresponding to that number is pressed. Available IC in 74 series is 74147 which is a priority encoder. This IC has active low inputs and outputs. The meaning of the word priority can be understood from the truth table. For example if 2 & 5 are low, the output will be corresponding to 5 which has a higher priority than 2 i.e. the highest numbered I/P has priority over lower numbered input's.

Truth table of 74147

Active low decimal input`s									**Active low BCD outputs**			
1	2	3	4	5	6	7	8	9	D	C	B	A
1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0
X	0	1	1	1	1	1	1	1	1	1	0	1
X	X	0	1	1	1	1	1	1	1	1	0	0
X	X	X	0	1	1	1	1	1	1	0	1	1
X	X	X	X	0	1	1	1	1	1	0	1	0
X	X	X	X	1	0	1	1	1	1	0	0	1
X	X	X	X	1	1	0	1	1	1	0	0	0
X	X	X	X	X	X	X	0	1	0	1	1	1
X	X	X	X	X	X	X	X	0	0	1	1	0



Q.57 What is a flip-flop? Write the truth table for a clocked J-K flip-flop that is triggered by the positive-going edge of the clock signal. Explain the operation of this flip-flop for the following conditions.
Initially all inputs are zero and assume the 'Q' output to be 1. **(10)**

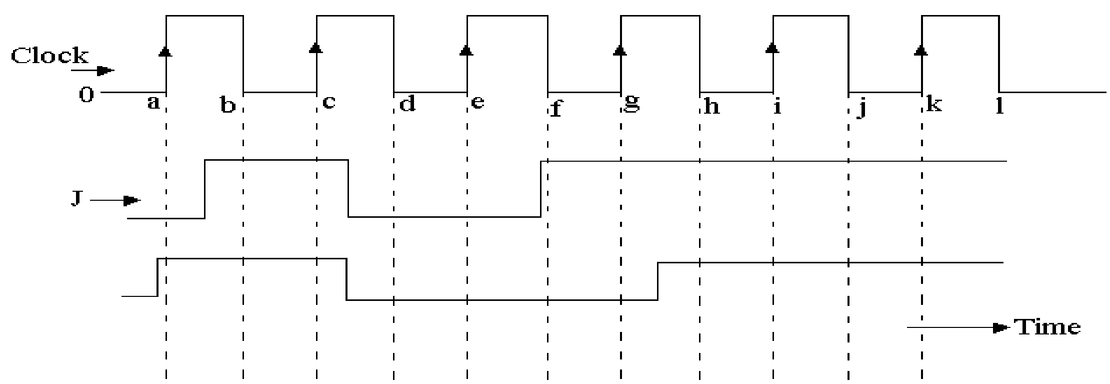


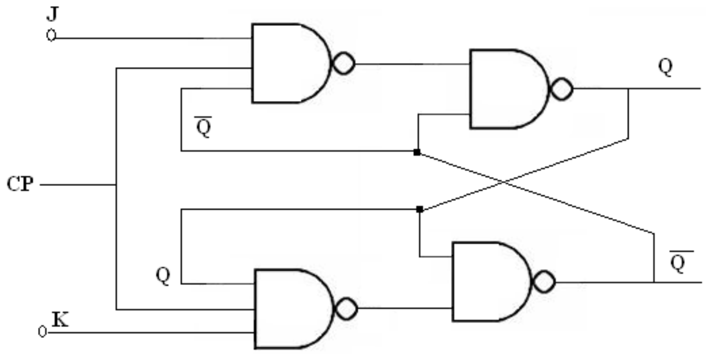
Fig.2

Ans:

Flip –flop is single bit memory cell. It stores single bit information in its true and compliment form. This is the fundamental block of any sequential circuit.

Truth table for clocked J K Flip- flop

clock	J	K	Q(t+1)
0	X	X	Q(t)
1 (rising edge from 0) 0 → 1	0	0	Q(t)
-do-	1	0	1
-do-	0	1	0
-do-	1	0	Q`(t)



J K flip flop

Let Q = 0 initially

At 1st (1) edge Q = 0

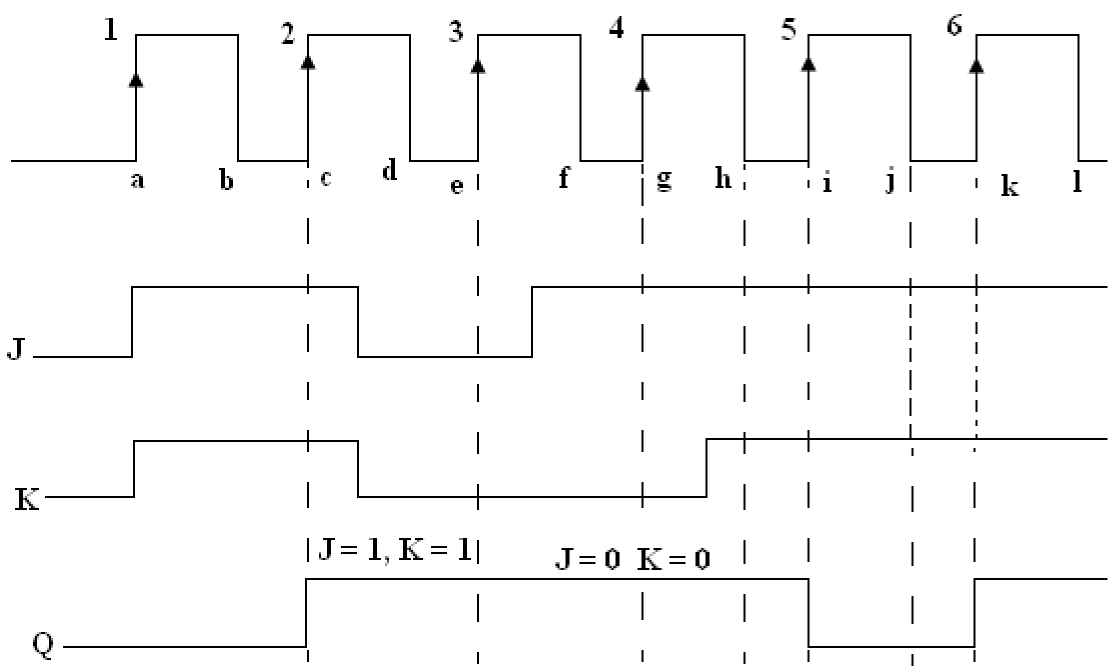
At 2 nd (2) edge J = 1, K = 1 ⇨ Q = 1

At 3 rd (3) edge J = 0, K = 0 ⇨ Q = 1

At 4 rth (4) edge J = 1, K = 0 ⇨ Q = 1

At 5 th (5) edge J = 1, K = 1 ⇨ Q = 0

At 6 th (6) edge J = 1, K = 1 ⇨ Q = 1



Q.58 How is it possible to make a modulo 2^n counter using N-flipflops? Name the two types of such counters. **(4)**

Ans:

Module 2^n counter counts total 2^n distinguishable states we know that n-bit can represent 2^n unique combinations for eg. Mod-8 counter will count total 8 states and as $8=(2^3)$ each state will have combination of 3 bits.

Two types of such counters are:

- Mod 8 counter
- Mod 16 counter

Q.59 In applications where the required memory capacity cannot be satisfied by a single available memory IC chip, what should the designer do to meet this requirement? **(10)**

Ans:

If the single memory chip can not be specified the required memory capacity then the designer should do the followings.

(1) Find out the no of single chip required to full fill the total capacity by

$$\text{No of chip} = \frac{\text{Required capacity}}{\text{Available capacity}}$$

(2) There are two type of expression

(i) Increasing memory location or words

(ii) Increasing word size, i.e. no of bits in each word.

(3) In case (i) the number will be of same as the address lines of available chip. The difference of the address lines of the capacity 7 availability will give the size of the decoder and the output of the decoder will decode among the chips.

In case (ii) address line data lines will be common to all chips because all chips at the same location collectively make a single word.

Q.60 Explain the operation of 8:1 multiplexer. **(8)**

Ans:

There are 8 Inputs & 1 Output and three select lines S2, S1, S0. Any one of the inputs will be selected & transmitted to the output depending upon the combination of the select lines, for e.g. If $S_2S_1S_0 = 001$ then information present on I1 line will be transmitted to the output.

Q.61 What is race around condition? How it can be avoided? **(8)**

Ans:

Race Around Condition:-

Jn	Kn	Q(n+1) output
0	0	Q(n)
1	0	1
0	1	0
1	1	Q(n)'

In JK flip-flop, When J=k=1 then output will be the complement of the previous state. Suppose the output Q_n is 0 and clock pulse is high. After the time interval Δt equal to the propagation delay through two NAND gates the output will change to the Q_{n+1}=1 (if J=K=1). Now we have=K=1 and Q=1 and after another Δt interval the output, Q will change to 0 from 1. Hence after every Δt duration of the output will flip between 0 and 1. At the end of the clock pulse the value of Q is uncertain because the value of Δt is not known exactly. This situation is known as race around condition .

The race around condition can be avoided if

1 Duration of clock pulse being high is small as compare to the delay of the gates. This is difficult because of very small propagation delay in IC's.

2 A master slave JK flipflop is used. In this 2 SR flip-flops are there. The feedback from the output of the second to the input of the first flip-flop. Positive clock pulses are applied to the first clock pulse and clock pulse are inverted at the second flip-flop when clk=1 first flip-flop is enabled and second is disabled clk'=0.

Q.62 Draw the circuit diagram of Asynchronous decade counter and explain its working. **(8)**

Ans:

To design a decade asynchronous counter first we draw the circuit for MOD 16 asynchronous counter which counts from 0 to 15 using four flip-flop (JK or T flipflop). It should count from 0 to 9 and then come to 0. The first state to be skipped is 1010 (10)here Q_3 and Q_1 are 1 and Q_2 and Q_0 are 0 if we take Q_3 and Q_1 and applied these to a NAND gate then the output of the NAND gate will be low only where Q_3 and Q_1 are high. This signal can be used to asynchronously clear all flipflops to make the counting state 0000. In this way MOD 16 counter will be restricted to count 10 state that is from 0 to 9.

Q.63 Explain the following for an ADC

(i) Input stage. (ii) Resolution.

(iii) Accuracy. (iv) Quantization error. **(8)**

Ans:

(i) Input Stage- In A-D Converter at the input stage, analog voltage can have any value in a range but the digital output can have only 2^N discrete values for an n bit A-D converter.

(ii) Resolution- This is the smallest possible change in input voltage as the fraction of percentage of the full scale output range.

(iii)Accuracy-The accuracy of D/A converter is the difference between actual output voltage and the expected output voltage in D/A converter.

(iv)Quantization error- An analog voltage is in the range of 0 to 1V and for 3 bit output, the size of each interval is S=1/8.Each interval is assigned a 3 bit binary value .We observe that the

whole range of voltage in an interval is represented by only one digital value .This error is referred to an quantization error which is because of process of quantization.

Q.64 Give the details of excess 3 code and gray code using four binary digits. Compare the two codes. **(8)**

Ans:

Binary no	Excess3	Gray code
0 0 0 0	0 0 1 1	0 0 0 0
0 0 0 1	0 1 0 0	0 0 0 1
0 0 1 0	0 1 0 1	0 0 1 1
0 0 1 1	0 1 1 0	00 1 0
0 1 0 0	0 1 1 1	0 1 1 0
0 1 0 1	1 0 0 0	0 1 1 1
0 1 1 0	1 0 0 1	0 1 0 1
0 1 1 1	1 0 1 0	0 1 0 0
1 0 0 0	1 0 1 1	1 1 0 0
1 0 0 1	1 1 0 0	1 1 0 1
1 0 1 0		1 1 1 1
1 0 1 1		1 1 1 0
1 1 0 0		1 0 1 0
1 1 0 1		1 0 1 1
1 1 1 0		1 0 0 1
1 1 1 1		1 0 0 0

Excess 3 Code

1. It is another from of BCD code. Each decimal digit is coded in 4 bit binary code.
2.The code for each decimal digit is obtained by adding decimal 3 to the natural BCD code of the digit.
3.The code is obtained by adding 3 to the decimal no
4.Self complementing code-useful in subtraction.

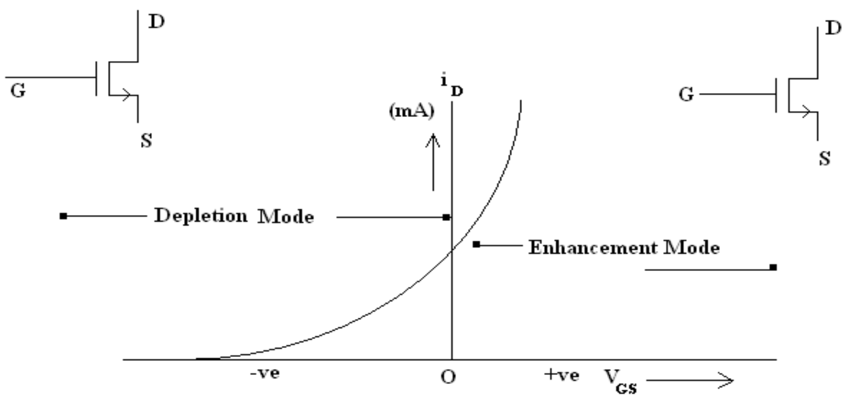
Gray Code

1. Very useful code. Also called reflected code.
2. Each gray code differs from the preceding and succeeding codes by a single bit.
3. Used in shaft encoders.

Q.65 Distinguish between enhancement mode and depletion mode metal oxide semiconductor field effect transistors giving their characteristics. **(6)**

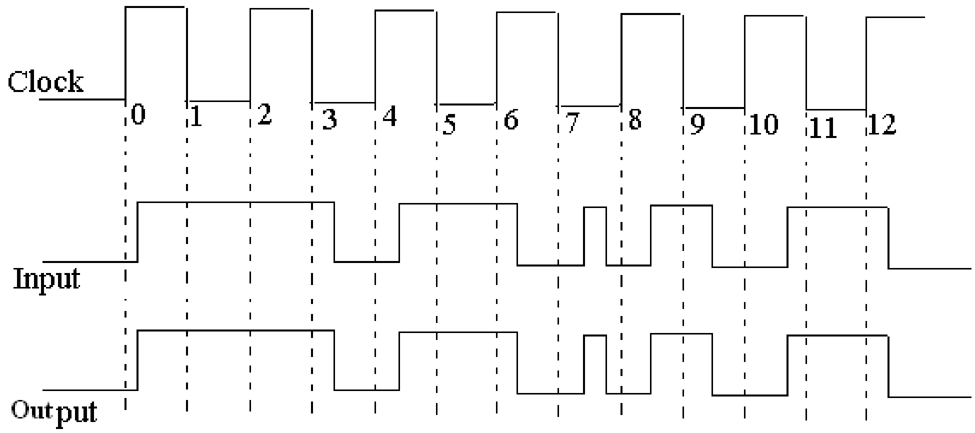
Ans:

E Mode MOSFET	Depletion Mode MOSFET
01. No channel exists between rain and source at $V_{GS} = 0$	01. Channel exists at $V_{GS} = 0$ [in fabrication n type impurity is diffused between two n+ regions
02. Threshold voltage is positive for nMOS Device.	02. Threshold voltage is negative for nMOS Device.
03. No current flows for negative V_{GS} [nMOS]	03. Current flows even for negative V_{GS}



Q.66 The clock and the input waveforms shown below are applied to the D input of a positive edge triggered D flipflop. Sketch the output waveforms. **(6)**

Ans:



As it is D Flip Flop at the positive edge ,output will be same as the input.

Q.67 What are the specifications/ characteristics used by the manufacturers to describe a digital to analog converter. Explain each one briefly. **(8)**

Ans:

The characteristics of D/A converter are

(i)Resolution:- This is the smaller possible change in output voltage as a function of percentage of full scale output voltage.

(ii) Linearity:-In a D/A converter equal increments in the numerical significance of the digital circuit the input-output relationship is not linear.

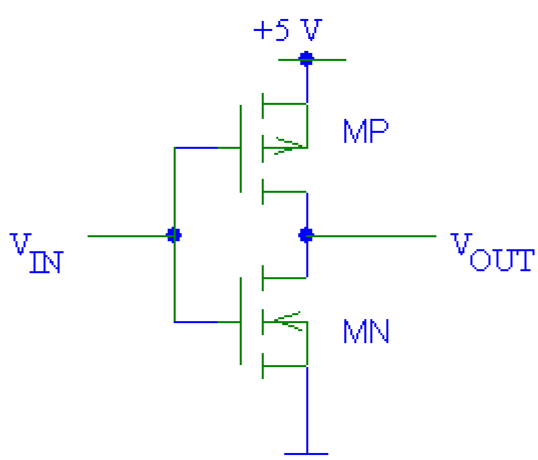
(iii)The accuracy of D/A converter is a measure of the difference between the actual output voltage and the expected output voltage.

(iv) Settling time:-when the digital input to a D/A Converter changes the analog output voltage does not change absolutely. Because of the presence of switches, active devices, stray capacitances and inductances associated with passive circuit components. The transient appears in the output voltages and oscillations may also occur the time required for the analog output to settle within +- ½ LSB of the final value after a change in the digital input is known as settling time.

Q.68 Describe CMOS inverter and state advantages of CMOS. **(8)**

Ans:

CMOS inverters (Complementary MOSFET Inverters) are some of the most widely used and adaptable MOSFET inverters used in chip design. They operate with very little power loss and at relatively high speed. Furthermore, the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large.A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage V_{DD} at the PMOS source terminal, and a ground connected at the NMOS source terminal, were V_{IN} is connected to the gate terminals and V_{OUT} is connected to the drain terminals.(See diagram). It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient that a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS and PMOS varies accordingly. If we model each transistor as a simple switch activated by V_{IN}, the inverter's operations can be seen very easily:

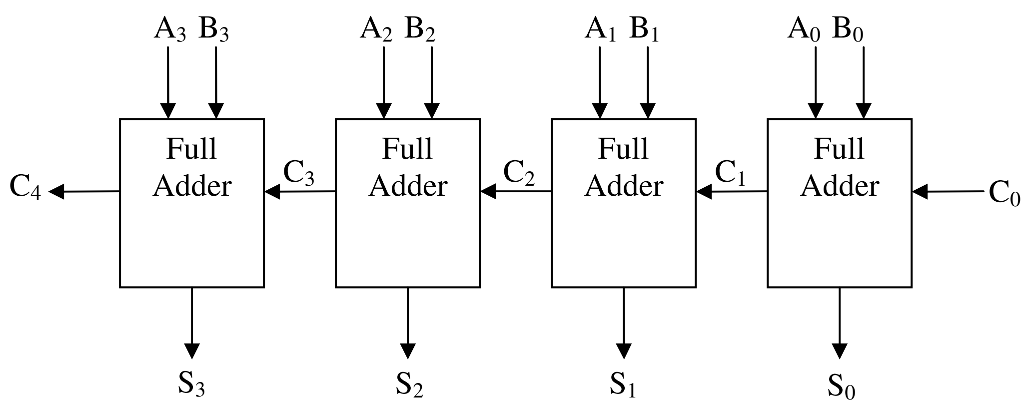


Following are the advantages of CMOS:

- Both n-channel & p-channel devices are fabricated on the same substrate.
- Low power dissipation, so more efficiency.
- Good noise immunity.
- High packing density.

Q.69 What is parallel adder? Draw and explain block diagram for 4 bit parallel adder. **(8)**

Ans:
By using full adder circuit, any two bits can be added with third input as carry. If numbers of bits are more than one, then full adder circuits are cascaded. Addend & Augend bits are applied simultaneously at inputs to the full adders. Carry generated in the lower significant stage is transferred to the next higher stage so that it can be added there.



Q.70 What is parity generator and checker? Describe five bit even parity checker. **(8)**

Ans:
When a digital signal is transmitted, it may not be received correctly by the receiver. At the receiving end it may or may not be possible to detect the error. To overcome this problem, an extra bit is attached to the n-bit code word to make the number of bits (n+1) in such a way so as to make the number of ones in the resulting (n+1) bit code even or odd. Then it will be an error detecting code. So for detection of error this extra bit is known as parity bit. Parity term is used to specify the number of ones in a word as odd or even. A logic circuit that checks the parity of a binary word is called as parity checker. Similarly a logic circuit that generates an additional bit to make the digital word of desired parity (even or odd) is known as parity generator.

Five bit even parity checker:

EX-OR gates are used for checking the parity as they produce output 1, when the input has an odd number of 1's. Therefore an even parity input to an EX-OR gate produces a low output.

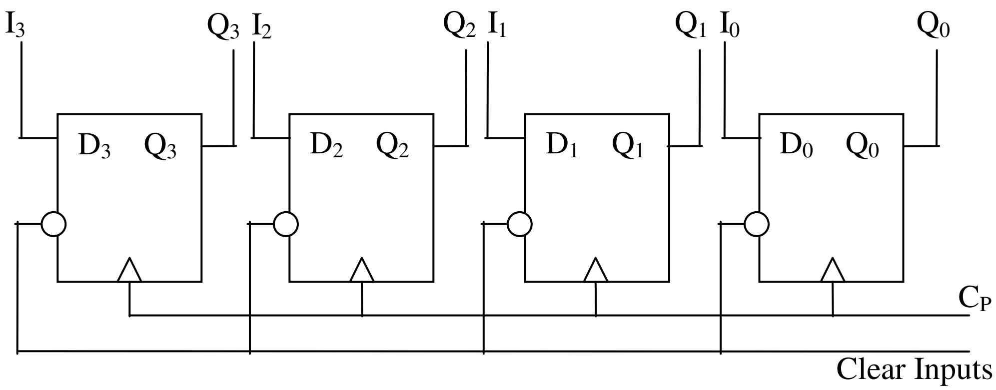
Truth table

W	X	Y	Z	P	C
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	1

Q.71 Describe the operation of parallel in parallel out (PIPO) shift register. **(8)**

Ans:

Parallel In Parallel Out



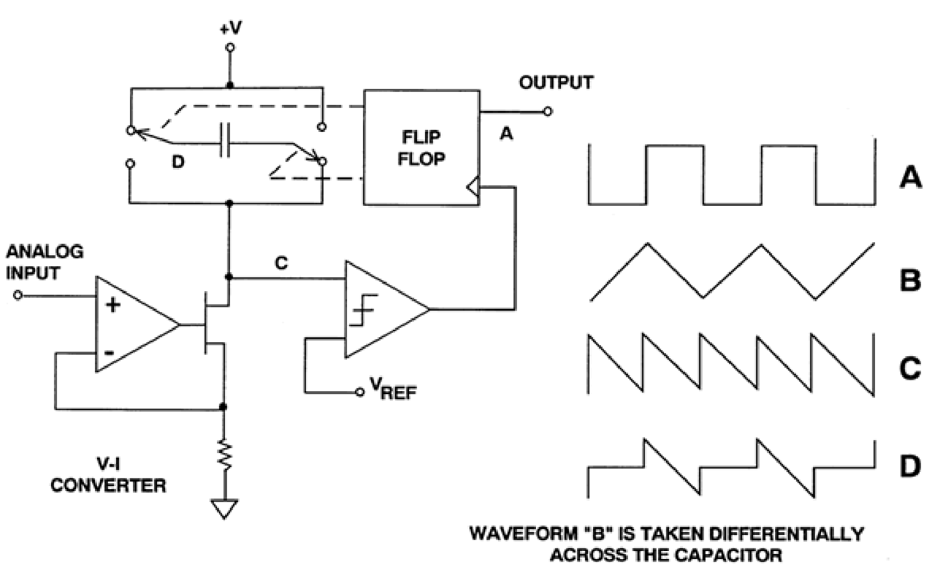
As the name suggests, in parallel in parallel out (PIPO), inputs are given in parallel, and outputs are also taken in parallel fashion. For synchronization same clock pulse is connected to all flip-flops. Thus any state change will take place simultaneously. Clear inputs are also connected to all flip-flops. So that the register can be cleared if required.

Q.72 Describe the operation of voltage to frequency ADC. **(8)**

Ans:

A voltage-to-frequency converter (VFC) is an oscillator whose frequency is linearly proportional to a control voltage. The VFC/counter ADC is monotonic and free of missing codes, integrates noise, and can consume very little power.

The current-steering multivibrator VFC is actually a current to-frequency converter rather than a VFC, but, as shown in Figure below, practical circuits invariably contain a voltage to-current converter at the input. The principle of operation is evident: the current discharges the capacitor until a threshold is reached, and when the capacitor terminals are reversed, the half cycle repeats itself. The waveform across the capacitor is a linear triangular wave, but the waveform on either terminal with respect to ground is the more complex waveform shown.



A_3	A_2	A_1	A_0	d_6	d_5	d_4	d_3	d_2	d_1	d_0	I	x
-	-	-	-	-	-	-	-	-	-	-	---	-
0	0	0	-	-	-	-	-	-	-	0	I	0
0	0	0	-	-	-	-	-	-	-	1	I	1
0	0	1	-	-	-	-	-	-	0	-	I	0
0	0	1	-	-	-	-	-	-	1	-	I	1
0	1	0	-	-	-	-	-	0	-	-	I	0
0	1	0	-	-	-	-	-	1	-	-	I	1
0	1	1	-	-	-	-	0	-	-	-	I	0
0	1	1	-	-	-	-	1	-	-	-	I	1
1	0	0	-	-	-	0	-	-	-	-	I	0
1	0	0	-	-	-	1	-	-	-	-	I	1
1	0	1	-	-	0	-	-	-	-	-	I	0
1	0	1	-	-	1	-	-	-	-	-	I	1
1	1	0	-	0	-	-	-	-	-	-	I	0
1	1	0	-	1	-	-	-	-	-	-	I	1

Q.73 Draw and explain the function of dual slope analogue to digital converter. Derive the equations used. **(8)**

Ans.

Dual slope A to D converter: It has 4 major blocks.

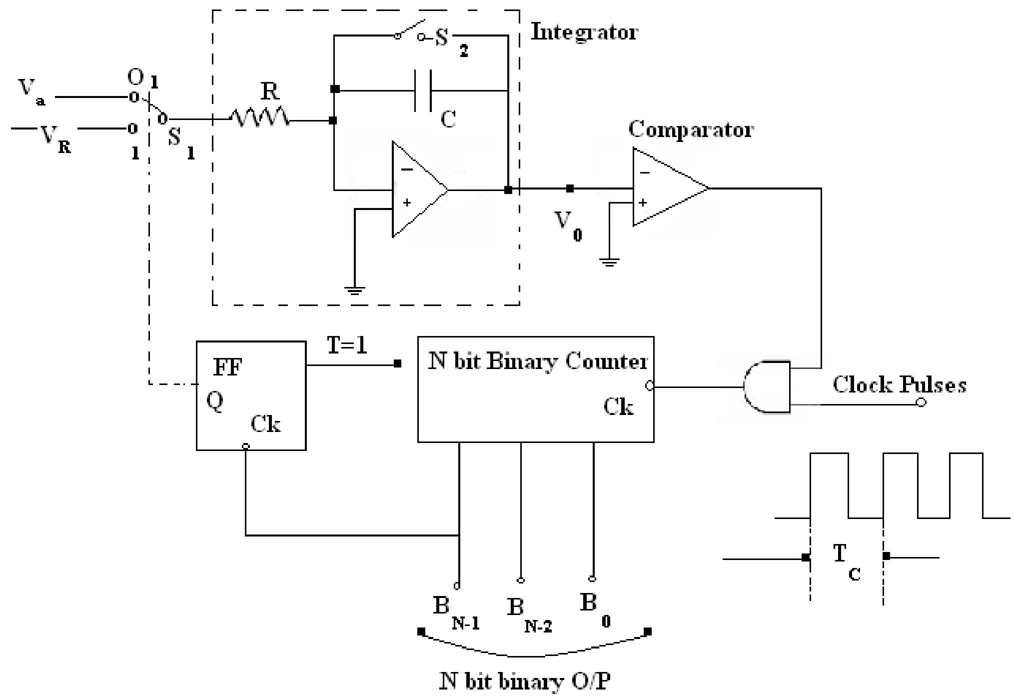
1. An integrator
2. A Comparator
3. A binary counter
4. A switch driver

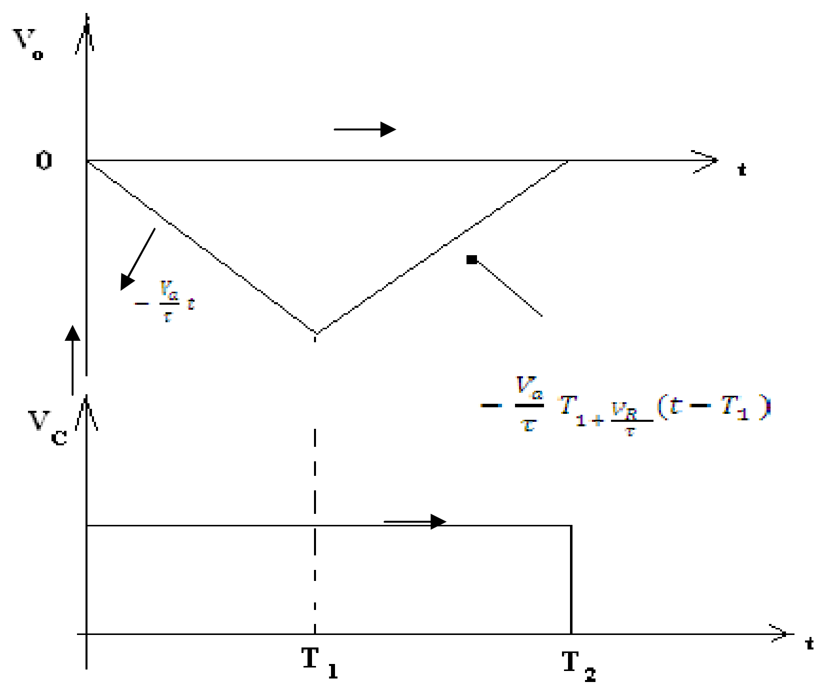
The conversion process at T=0 with switch S1 in position 0. This connects the analogue voltage Va to the input of the integrator. The output of the integrator will be

$$V_0 = -\frac{1}{\tau}\int_0^t V_a\,dt = -\left[\frac{V_a}{\tau}\right]t$$

This results in high V_c. This enables the AND Gate and the clock pulse reaches the ck input of the counter, which was initially clear. The counter counts from 00……00 to 11…..11 when

$2^n - 1$ clock pulses are applied. At the next clock pulse 2^n the counter is cleared and Q becomes 1. This controls the state of S_1 which now moves to position 1 at T_1, thereby connecting $-V_R$ to the input of the integrator. The output of the integrator now starts to move in the positive direction. The counter continues to count until V_0 is less than 0. As soon as V_0 goes positive at T_2, V_C goes LOW disabling the AND Gate.





Wave form of dual slope A/D convertor

The time T1 is given by

$T_1 = 2^N T_C$ where T1 is time period of clock pulse.

When the switch S1 is in position 1, the output voltage of the integrator is given by

$$V_0 = -\frac{V_a}{\tau} T_1 + \frac{V_R}{\tau}(t - T_1)$$

$V_0 = 0$ at $t = T_2$

Therefore, $T_2 - T_1 = \frac{V_a}{V_R} T_1 = \frac{V_a}{V_R} 2^N T_C$

Let the count recorded in the counter be n at T_2 therefore $T_2 - T_1 = n\,T_C = \frac{V_a}{V_R} 2^N T_C$

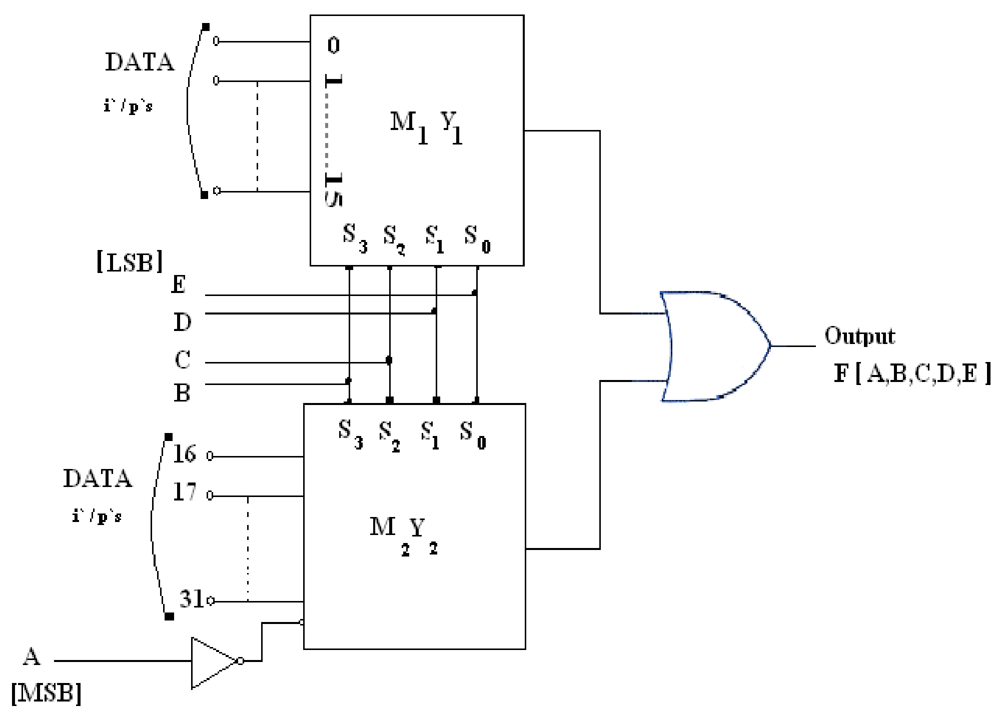
which gives $n = \frac{V_a}{V_R} 2^N$

Q.74 What is a Multiplexer Tree? Why is it needed? Draw the block diagram of a 32:1 Multiplexer Tree and explain how input is directed to the output in this system.**(10)**

Ans

Multiplexer Tree: The largest available MUX IC is 16 to 1. To meet the larger input needs there should be a provision to expand it. This can be achieved with the help of Strobe Inputs and so MUX trees are designed.

One of the possible method is shown for 32 to 1 MUX, by using two 16 to 1 MUX and OR Gate.

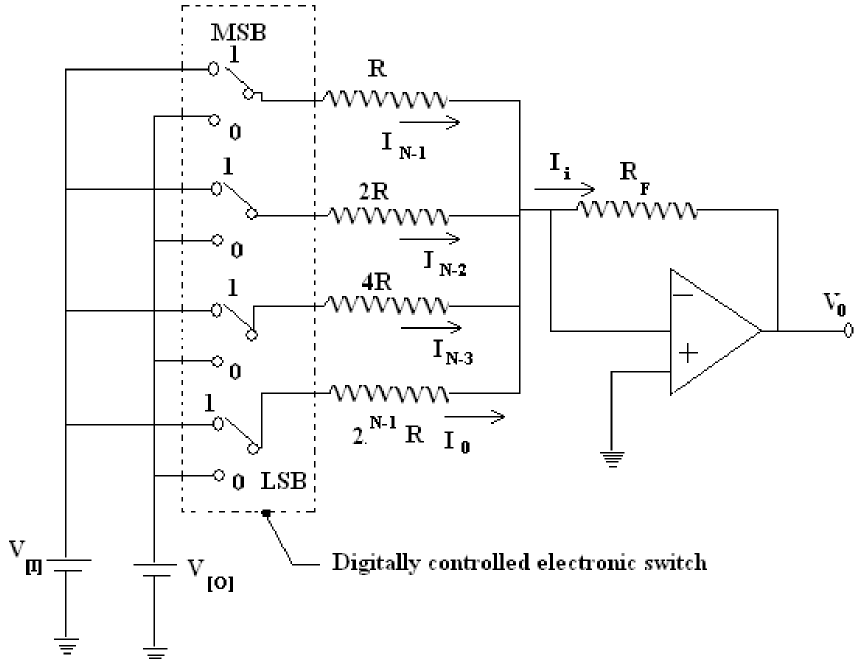


There are two 16 to 1 MUX M_1 and M_2 having data inputs 0…..15 and 16…..31 respectively. The selection lines are S_3 S_2 S_1 S_0 , which are able to select one input among 16 inputs. Now the strobe pin is used as fifth selection line that is if it is 0 than one input among the upper MUX is selected and if A = 1, than one among the data input of lower MUX is selected. The output of both the MUX are O Red.

Q. 75 With the help of a neat diagram, explain the working of a weighted-resistor D/A converter. **(9)**

Ans

Weighted Register D/A



Converter:

N Bit digital input is applied to a register network through electronic switch. This electronic switch produces current I at MSB (corresponding to Logic 1), I/2 at the next lower significant position. The total current produced will be proportional to digital input. This current can be converted to corresponding voltage by using an op-ampere. This circuit is referred to as weighted register converter since the resistance values are weighted in accordance with the binary weights.

The current I_i is given by

$I_i = I_{N-1} + I_{N-2} + \ldots\ldots + I_0$ where $I_{N-1} = V_{N-1}/R$, $I_{N-2} = V_{N-2}/2R$, $I_{N-3} = V_{N-3}/4R$

also $V_N = V(1)$ if bn = 1, V(O) if bn = 0

For straight binary inputs V(0) = 0 and V(1) = - V_R and the output voltage is given by

$$V_0 = -[-V_R]\left[\frac{R_F}{R}b_{n-1} + \frac{R_F}{2R}b_{n-1} + \frac{R_F}{2^2R}b_{n-1} + ________ + \frac{R_F}{2^{n-1}R}b_0\right]$$

Q. 76 Briefly explain the following:

(i) Binary number system.

(ii) Signed binary numbers **(7)**

Ans

(i) Binary Number System

The number of system with base or Radix two is known as the Binary Number System. To represent the number, 0 & 1 are used. These are known as bits. It is a positional system that is every place carries specific weight. As the base is two, the coefficients can take only two value i.e. 0 & 1.

$$(N)_b = d_{n-1}\, d_{n-2} \ldots\ldots\ldots d_0 * d_{-1}\, d_{-2} \ldots\ldots\ldots d_{-m}$$

integer portion   Radix Point   Fraction

b = 2 (Radix)

d_{n-1} = Most significant bit

d_{-m} = Least significant bit

& $.0 \le (d_i \text{ or } d_{-f}) \le b_{-1}$

(ii) Signed Binary Numbers: In decimal number system positive numbers are denoted by (+) sign and negative numbers are denoted by –ve sign Digital circuits understand only the language of 0`s and 1`s. Thus normally an additional bit is used for sign and it is placed at the most significant position.

1. A `O` is used for +ve nos. and 1 is for –ve numbers. For example an eight bit signed number 00000100 represents +4 and 10000100 represents (-4). This representation is known as sign magnitude number. There are three different ways by which signed numbers are presented.
2. **One's compliment representation:** In this system the +ve numbers are represented by their Binary equivalent with a 0 placed at most significant position to represent the –ve numbers compliment is taken and than a `1` is placed as MSB to represent the –ve sign. For example $+ 7 = (0111)_2$

   $- 7 = (1000)_2$
3. **Two's Compliment presentation**: If 1 is added number is known as I`s compliment of the binary No. For example 2`s compliment representation of 0101 is 1011. Since 0101 represents $(+5)_{10}$ therefore 1011 represents $(-5)_{10}$ in two's compliment representation.

Q.77 What is chattering as applied to mechanical switches used in digital systems and why do they occur? What is its effect on the functioning of a sequential circuit? **(6)**

Ans

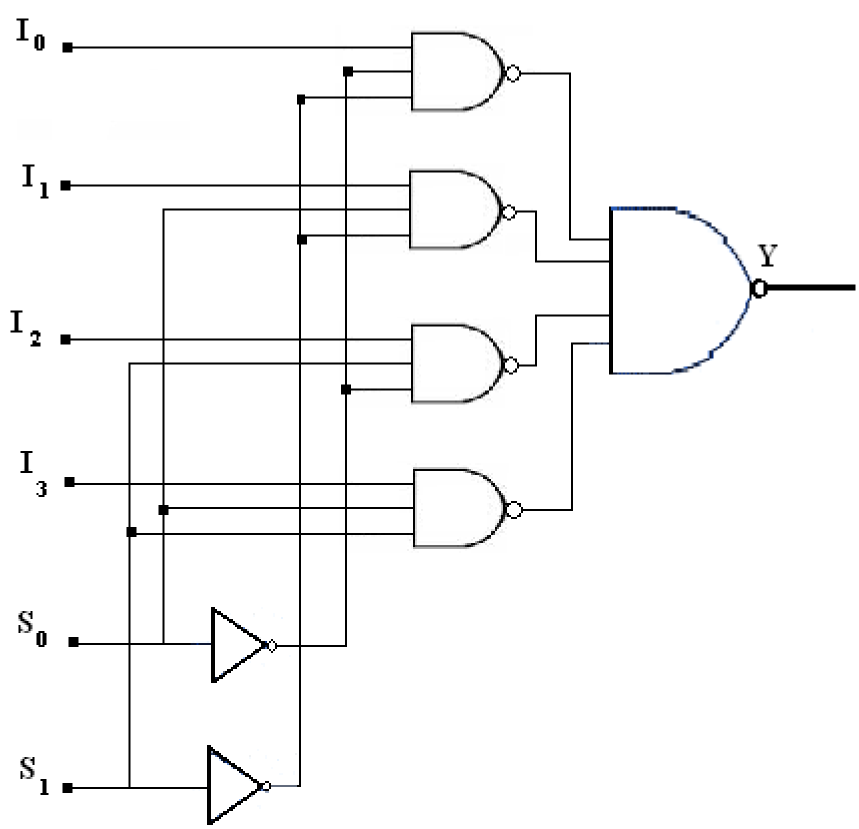
Chattering:

Mechanical switches are employed in digital systems as input devices by which digital information (0 or 1) is entered into the system. When the arm of the switch is thrown from one position to another, it chatters or bounces several times before finally coming to the root in the position of contact. This is known as bouncing or chattering. This bounce is result of the spring loaded impact of the switch through contact and the pole

contacts. In a sequential circuit, if a 1 is to be entered through a switch then the switch is thrown to the corresponding position, as soon as it is thrown to this position, the output is 1 but the output oscillates between 0 & 1 for some times due to make and break (bouncing) of the switch at the point of contact before coming to rest. This changes the output of the sequential circuit and creates difficulties in the operation of the system. This problem is eliminated by using bounce – free elimination switches

Q.78 Design a 4 : 1 multiplexer with strobe input using NAND gates. **(5)**

Ans



Design of 4 : 1 multiplexer with strobe input using NAND gates.

Q.79 Explain the operation of octal to binary encoder. **(8)**

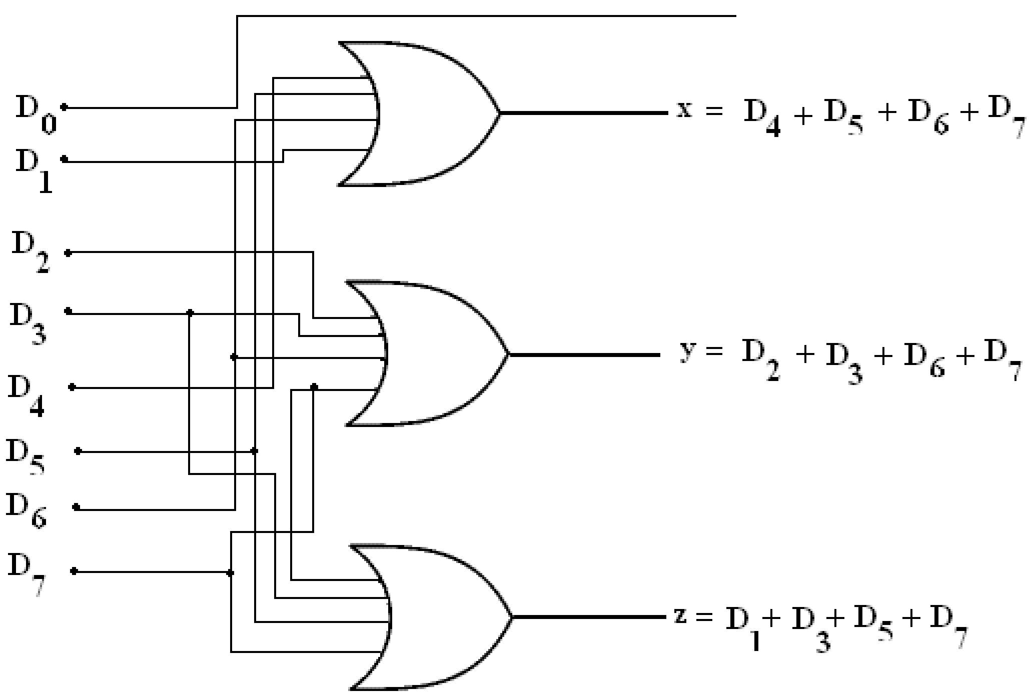
Ans

Octal to binary encoder consists of eight inputs, one for each of eight digits and three outputs that generate the corresponding binary number. For example: low order output bit Z is if the input octal digit is odd.

Here D_O input is not connected to any O R gate; the binary output must be all zeroes in this case and all 0's output is also obtained, when all inputs are zeroes. This discrepancy can be resolved by providing one more output to indicate the fact that all inputs are not zeroes.

Truth table

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



Logic diagram of octal to binary encoder